Five-Level One-Capacitor Boost Multilevel Inverter

Abdullah Mohammed Muneer[1], D. Karuna[2]
[1]*U.G. Student, Department of Electrical and Electronics Engineering, Vaageswari College of Engineering*
[2]*Assistant Professor, Department of Electrical and Electronics Engineering, Vaageswari College of Engineering*

***Abstract*—Multilevel inverter (MLI) configurations are increasingly recognized as the optimal choice for medium and high-power industrial applications. This study proposes a novel single-phase, five-level boost multilevel inverter architecture designed to generate a staircase output voltage with levels (2Vdc, Vdc, 0, −Vdc, −2Vdc). The hardware footprint is significantly optimized, requiring only one DC source, eight power switches, and a single capacitor. To achieve its unique boosting ability, the system operates based on "charge-pump theory," wherein the capacitor charges in parallel with the source and discharges in series to synthesize an output voltage that is higher than twice the input voltage. Control is managed via a level-shift pulse width modulation (LS-PWM) strategy, comparing a sinusoidal reference against four triangular carriers. Performance is validated through MATLAB/Simulink, demonstrating a compact design, reduced harmonic profile, and simplified control requirements.**

I. INTRODUCTION

Contextual Background DC to AC conversion is a cornerstone of modern renewable energy systems, which demand high-quality AC outputs with precise amplitude and frequency control. Pulse Width Modulation (PWM) inverters, ranging from traditional two-level to advanced multilevel configurations, serve as the primary interface for these energy sources. Comparative Analysis Conventional two-level inverters are hindered by high harmonic distortion and significant voltage stress on semiconductor components. Multilevel Inverters (MLIs) mitigate these issues by synthesizing a staircase waveform from multiple DC levels. While increasing the number of levels enhances power quality, it typically introduces a trade-off: increased hardware complexity, higher costs, and reduced reliability due to the proliferation of switches and driving circuits.

Literature Gap Established MLI topologies present several technical hurdles:

- Neutral Point Clamped (NPC):

Introduced by Akira Nabae and Akagi, this topology faces critical concerns regarding the stability and balancing of DC-link capacitors.

- Flying Capacitor (FC):

While offering phase redundancies that assist in fault tolerance, these systems suffer from control complexity and poor switching efficiency.

- Cascaded H-Bridge (CHB):

This modular design is effective but requires multiple independent DC sources, which increases system weight and cost.

- Modular Multilevel Converters (MMC):

These are prone to internal circulating currents and high conduction losses, with capacitor balancing remaining a primary control challenge.

Project Objective

This research aims to implement a five-level inverter that overcomes these limitations by utilizing only one DC source and one capacitor. A key advantage of this proposed configuration is its distinct boosting ability; unlike traditional topologies, this system allows the output voltage to reach levels higher than twice the input voltage, significantly enhancing its utility for low-voltage renewable sources.

II. POWER ELECTRONICS AND CONVERTER TOPOLOGIES

System Classification
Power electronic systems are classified by their conversion function: AC to DC (rectifiers), DC to AC (inverters), DC to DC (choppers/converters), and AC to AC (cycloconverters/regulators). The performance of these systems is governed by the switching characteristics of active semiconductor devices, including MOSFETs, IGBTs, and SCRs. Inverter Fundamentals Voltage Source Inverters (VSI) provide a controlled AC voltage from a constant DC link.

- Single-Phase Half-Bridge:

Suited for low-voltage applications, this configuration requires two large capacitors for filtering to prevent source short-circuiting during switching transitions.

- Single-Phase Full-Bridge:

This architecture utilizes an additional leg to allow the maximum output amplitude to reach the full input voltage (Vi), effectively doubling the capacity of the half-bridge.
Fig 2.2: Single-Phase Half Bridge Voltage Source Inverter Fig 2.3: Single-Phase Voltage Source Full Bridge Inverter DC to DC Conversion The proposed system integrates DC-DC step-up logic.
Conventional Buck converters act as step-down mechanisms, while Boost converters act as step-up mechanisms. The proposed system utilizes a switched-capacitor cell to facilitate voltage elevation within the inversion stage itself.

III. PROPOSED FIVE-LEVEL BOOST INVERTER SYSTEM

Architecture The proposed single-phase configuration utilizes eight power switches (S1– S8) and a single capacitor. This streamlined design eliminates the need for multiple isolated DC sources (as required by CHB) or clamping diodes (as seen in NPC), leading to a higher power density and lower cost.

Operational Theory
The system is governed by Charge-Pump Theory. The primary challenge in capacitor based MLIs is voltage balancing; this system addresses this by ensuring the capacitor is connected in parallel with the DC source during specific switching intervals to maintain its charge. During the boost phases, the capacitor is reconnected in series with the DC source, effectively adding $V_{dc} + V to achieve the $2V_{dc}$ level. Fig 1.1: Block Diagram of Five-Level One-Capacitor Boost Multilevel Inverter Operating Modes

The inverter cycles through six distinct modes to generate the five-level output:

- Mode I (Positive Peak): Switches are configured to place the DC source and capacitor in series, outputting +2V_{dc}$.
- Mode II (Positive Level): The output is derived directly from the DC source ($+V_{dc}$).
- Mode III (Zero Level): The load is shorted through the switches to generate 0V.
- Mode IV (Negative Level): The DC source is connected to the load in reverse polarity (-V{dc).
- Mode V (Negative Peak): The DC source and capacitor are connected in series with reverse polarity to output 2V_{dc}.
- Mode VI (Transition/Charging State):

This is a critical mode where specific switches engage to connect the capacitor in parallel with the DC source, ensuring voltage stability and balancing through the charge-pump mechanism. Fig 7.1: Operation Modes I, II, and III Fig 7.2: Operation Modes IV, V, and VI

IV. MODULATION STRATEGY AND CONTROL LOGIC

PWM Implementation A Level-Shift PWM (LS-PWM) strategy is employed to generate the gate pulses for the eight switches. In this scheme, a high-frequency triangular carrier is vertically shifted into four distinct bands. These carriers are compared against a sinusoidal reference signal to determine the instantaneous switching state required to synthesize the five-level staircase.
Controller Features The system incorporates a PID control algorithm optimized for inverter dynamics. Unlike generic PID implementations, this project focuses on integral mode implementation to eliminate steady-state error in the output voltage. The time response characteristics are tuned to ensure

rapid recovery during load transients, maintaining the stability of the capacitor voltage across all operating modes.

Comparative Analysis of Modulation Techniques Feature Sinusoidal PWM (SPWM) Space Vector PWM (SVPWM) DC

Bus Utilization | Standard efficiency 15% higher utilization Harmonic Profile Good Excellent (Lower THD) Implementation Complexity Low (Linear comparison) High (Vector transformations)

Control Domain General VSI applications High-performance industrial drives.

V. SIMULATION METHODOLOGY

Software Environment Performance verification was conducted using

MATLAB/Simulink. The model utilizes discrete time power electronic blocks to simulate the high-frequency switching environment of the eight-switch network.

Logic Flow The simulation follows a modular signal flow:

1. Reference Signal Generation: Synthesis of the fundamental 50Hz sine wave.
2. Multicarrier Comparison: Real-time comparison of the reference against the four shifted carriers.
3. Pulse Logic Mapping: Translating comparison results into specific gate signals for S1–S8 based on the six operating modes.
4. Power Circuit Execution: Modeling the series-parallel transition of the capacitor and DC source.

VI. RESULTS AND DISCUSSION

Simulation Analysis

Technical analysis confirms that the inverter successfully synthesizes the five-level staircase waveform. The measured voltage levels were recorded at 2Vdc, Vdc, 0, −Vdc, and −2Vdc.

Simulation Results:

Output Voltage and Current Waveforms showing 5-level staircase pattern Efficiency and Harmonics The simulation results indicate a significant reduction in Total Harmonic Distortion (THD) compared to conventional two-level inverters. Furthermore, the "boosting ability" was verified; the charge pump mechanism effectively elevated the output voltage, with peak values reaching higher than twice the input voltage as predicted in the theoretical model. This confirms the effectiveness of the single-capacitor series parallel transition logic.

VII. CONCLUSION

This research successfully developed and validated a five-level one-capacitor boost multilevel inverter. By utilizing a unique charge pump strategy, the configuration achieves a peak output voltage higher than twice the input with a minimal hardware count of only eight switches. The system offers a compact physical footprint, simplified control via LS-PWM, and enhanced voltage balancing, making it an ideal candidate for low-voltage renewable energy integration.

ACKNOWLEDGEMENT

I wish to pay my sincere thanks to Dr. CH. SRINIVAS, Principal, Vaageswari College of Engineering, Karimnagar, for providing all the required facilities and his support during the Project Stage - 2. My heartiest and sincere gratitude to my Guide Dr. K. CHANDRAMOULI, Professor and Head of Department, Department of Electrical & Electronics Engineering, Vaageswari College of Engineering for providing me with all possible facilities for carrying out the project work in the department.

REFERENCES

[1] Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, 1981.

[2] W. Stillwell and R. C. N. Pilawa-Podgurski, “Flying capacitor multilevel converters and clamping techniques,” Journal of Power Electronics, vol. 12, 2012.

[3] E. Babaei and S. S. Gowgani, “A review of switched-capacitor multilevel inverters,” IEEE Transactions on Power Electronics, 2014.

[4] A. Muneer and D. Karuna, “Hardware implementation of switched-capacitor cell MLIs,” Vaageswari College Research *Reports*, 2024.