Low-Power Noise-Tolerant Domino Logic Design Using 7-nm FinFET Technology

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Abstract–A **Low-power and noise-immune domino logic architecture is designed and synthesized in the 7-nm predictive technology (FinFET) model. The proposed circuit includes a keeper transistor, clock controlled footer devices, a stacking mechanism and a semi-dynamic output stage to minimize the leakage current and to avoid the possibility of false switching at the dynamic node. To validate the proposed technique a 2-input domino OR gate is used since its parallel pull-down network is a critical leakage condition without inherent transistor stacking. Simulations are done in Cadence Spectre on a nominal 0.8 V supply, a temperature of 27 °C, a clock frequency of 10 GHz and an output load of 10 fF. The proposed design consumes 0.33 nW as compared to the already existing domino logic structures, which consumes 15% less power than the existing ones and it has nearly 10% better speed.**

Index Terms**—Domino logic, Low Power, Noise Immunity, Dynamic node, OR.**

I. INTRODUCTION

As technology scales, the development of integrated circuit has become compact, fast and energy efficient. When transistors are scaled down to the deep-nanometre region, however, there are short-channel effects, increased leakage current, process variability, less noise margins and reliability issues. All these constraints have posed a challenge to conventional planar CMOS technology to obtain simultaneously low power, high speed and reliable operation [1]–[4].
For advanced technology nodes, fin field-effect transistors (FETs) have become an alternative to planar MOSFETs. A FinFET has a better electrostatic control, lower subthreshold leakage, higher drive current, and better short channel effect suppression due to the gate constraining the channel from multiple side directions. The multiple side directions of the gate constrain the channel in the FinFET, resulting in better electrostatic control, lower subthreshold leakage, higher drive current, and better suppression of short channel effect [1, 4]. The structure of planar and FinFET devices are shown in Fig. 1. Such attributes have made FinFET technology a good choice for low-power memory cells, analogue circuits and high-speed digital circuits [6]–[10] respectively.

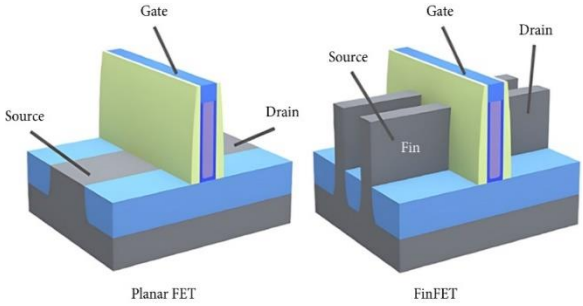

Figure 1: Comparative analysis of planar FET architecture and FinFET architecture

The style of logic used in a digital circuit is also greatly influential in its performance. Static CMOS offers maximum voltage swing, high noise immunity and low static-power dissipation. However, its complementary pull-up and pull-down networks result in an increase in the number of transistors used, input capacitance, and circuit area. Domino logic has reduced input capacitance and faster evaluation, and can be used for high-speed and wide fan-in logic functions. The charge that appears on its dynamic node, however, is subject to leakage current, charge sharing, capacitive coupling, clock feedthrough and noise disturbances [2, 5].
A keeper transistor is usually used to recover the charge which is lost from the dynamic node. An insufficient keeper can not protect the node well, while a strong keeper can cause the contention of pull down network and consume more power and propagation delay. This issue is worse for domino OR

gates since there is no stacking effect provided by the transistors that are connected in parallel to pull down. The leakage of parallel devices may cause the leakage of the dynamic node unintentionally and lead to an incorrect output.

In this work, a domino low power and noise-immune architecture of logic is proposed with 7-nm predictive technology model. Architecture is the combination of keeper and footer transistors, controlled stacking mechanism and semi-dynamic output stage. In this work, the general proposed architecture is shown and the realization of the OR-gate with two inputs and the corresponding schematic of 7 nm FinFET are presented. The power consumption, propagation delay, power–delay product, variation in supply–voltage, variation in temperature, and process variation are used to evaluate the design.

II. LITERATURE REVIEW

The studies of past years have examined the FinFET circuits with respect to process, voltage and temperature variations to ascertain its suitability for reliable low-power systems. PVT-aware modelling has shown that the supply voltage, temperature, threshold-voltage variation and device dimension all can have a significant impact on the delay and power consumption of the FinFET circuits [11]. There have also been comparative investigations of 7-nm FinFET and planar CMOS standard cells which have shown that the speed, leakage performance and parasitic effects in FinFET implementations are improved relative to planar CMOS as the dimensions are reduced [12]. For low-power applications, the switching-energy dissipation has also been investigated using the same approach as in [13] but with the addition of the use of FinFET-based adiabatic logic.

The traditional domino type structure with no feet as shown in Fig. 2 has a short assessment path and low delay. But it has no clock controlled footer which makes it more susceptible to leakage and charge sharing. The footed structure shown in Fig. 3 provides better isolation between the pull-down network and ground during precharge, however it has the drawback of having a higher value of footer resistance which results in a longer evaluation delay. To alleviate the leakage problem in high fan-in dynamic circuits, diode-footed domino logic was proposed, but the diode footed footer will decrease the discharge current [14].

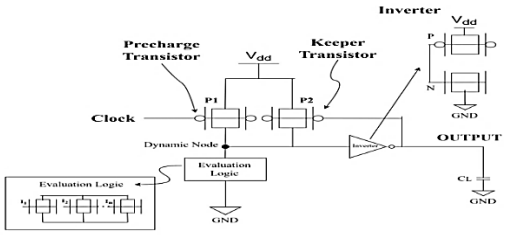

Figure 2: Domino logic architecture based on without foot (DLWF)

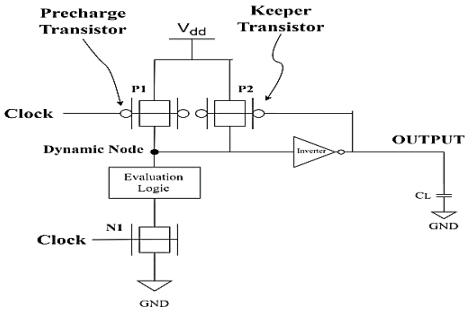

Figure 3: Domino logic architecture based on foot (DLF) [17]

The circuits using the keeper are more stable for dynamic nodes, because they compensate for leakage current. However, when there is conflict between the keeper and pull-down network, then there is an increase in delay and power. In order to achieve a better noise tolerance with a relatively low keeper strength, there are some noise-tolerant dynamic CMOS techniques that have been suggested using controlled clock and latching mechanisms [15]. There are also circuits developed that are leakage tolerant by modifying the evaluation and keeper paths; these circuits result in an area and timing overhead due to the additional transistors [16]. By incorporating a self-resetting logic circuit as in Fig. 4, very rapid successive evaluations can be realized, automatically resetting the dynamic node. However, a reset needs to be timed carefully so as not to reset too early or to give the wrong output. The cascaded structure in high speed in Fig. 5 enhances the cascading ability, but adds extra internal nodes that are susceptible to leakage and process variation. Reliability analysis of FinFET circuits has been verified that the device and operating parameter variation need to be taken into account in the design of a nanoscale high-speed circuit [17]. For these circuits, it is also necessary to

have validated compact models like BSIM-CMG model for multi-gate devices [18] to get an accurate simulation of the circuit.

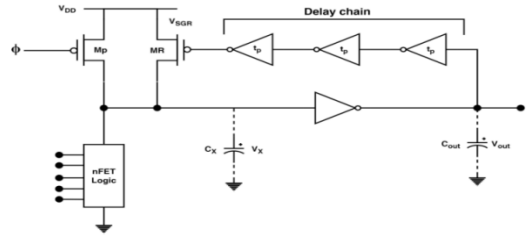

Figure 4: Domino logic based on self-resetting logic circuit(SLRC)

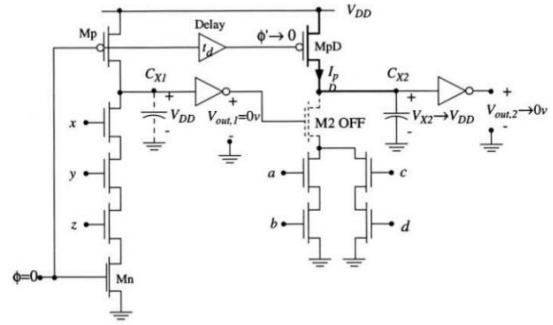

Figure 5: Domino logic based on High speed cascaded structure (HSCS)

Current approaches typically offer a better tradeoff on a specific aspect of the system, like leakage, delay or noise immunity, but at the cost of another. The robustness can be improved by having strong keeper devices but will make the system more competitive whilst the footer and stacking techniques will reduce the leakage but make the system slower to discharge. Proposed architecture thus incorporates the control by the keeper, foot assisted stacking and semi-dynamic buffering and achieves a balance in improvement of power consumption, propagation delay and noise tolerance.

III. PROPOSED LOW POWER DOMINO LOGIC CIRCUIT

The suggested low power and noise-immune domino structure are depicted in Fig. 6. It includes a precharge transistor made of PMOS, a pull down network made of NMOS transistors, a keeper transistor, NMOS footer devices controlled by clock, and a modified output inverter. For this reason, the keeper and footer arrangement is chosen to allow the discharge due to leakage to be minimized while not adding any contentions to the evaluation.

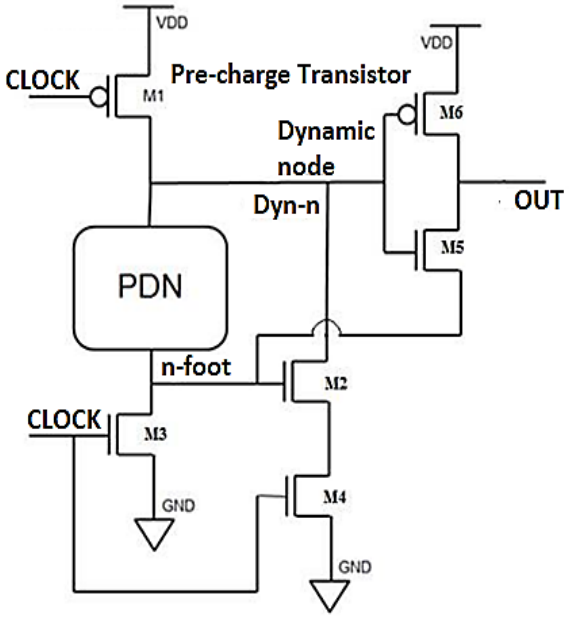

Figure 6: Proposed Low Noise Immune Low Power Domino logic architecture

In the precharge stage (when CLK is 0), transistor M1 is turned ON and precharges the dynamic node to V_DD. Evaluation path is disconnected from GND with the clock controlled evaluation path OFF. The charged dynamic node generates the output of low value in the inverter due to that charged dynamic node. The keeper transistor is included to hold the voltage of the dynamic node away from the subthreshold leakage and coupling noise.

If CLK = 1, M1 is turned OFF and the evaluation path is turned on. If the combination of inputs causes the pull-down network to be activated the dynamic node will discharge through the footer path. If not, the precharged voltage will be maintained. The stacked footer structure helps to compensate for the reduction of the gate-to-source voltage of the OFF devices and helps to reduce leakage through the pull-down network. This is an attractive solution in the case of wide fan-in domino circuits, where stability of the dynamic node is a major concern [2], [5], [14]–[17].

The schematic of the 7 nm FinFET implementation for the 2-input OR-gate is presented in Fig. 7. Aand Bare were connected to parallel NMOS devices, since

the requirement for an OR gate is the pull-down condition, A+B. This is an important condition for domino logic as there is no natural stacking effect when OFF transistors are in parallel.

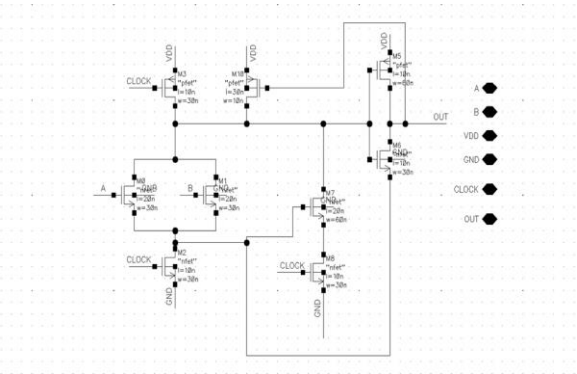

Figure 7 : Proposed Low Noise Immune Low Power Domino logic 2-input OR gate architecture in 7nm finFET technology

The controlled evaluation and footer path is made up of transistors M3-M5. The intermediate node (n-foot) is also connected to the source of NMOS transistor in the output stage. This semi-dynamic connection eliminates the possibility of the transition of the precharge state of the dynamic node being an unwanted output pulse. The keeper holds the charge and the stacked footer devices prevent uncontrolled charge discharge. The leakage power is therefore minimized and the noise is well tolerated in the proposed circuit with a relatively small increase in the evaluation delay.

IV. SIMULATION RESULTS AND DISCUSSION

The proposed circuit has been simulated in Cadence spectre with 7-nm PTM FinFET model. The nominal voltage and temperature supplied was maintained at 0.8 V and 27 °C, respectively. The frequency of the clock was 10 GHz, and the output load was 10 fF. Propagation delay between 50% transition points of input or clock and output wave form was measured. The same clock conditions, input activity and load capacitance conditions were used throughout the simulation of all the compared circuits to make a fair comparison.

This is confirmed by the transient response shown in Fig. 8 which shows that the two-input OR gate is working correctly. In the precharge period, the Dynamic node is charged and the output is low. In evaluation, logic 1 on either of the inputs turns on the pull down network, discharges the dynamic node and causes the output to go high. No undesired transition is seen at output at precharge time.

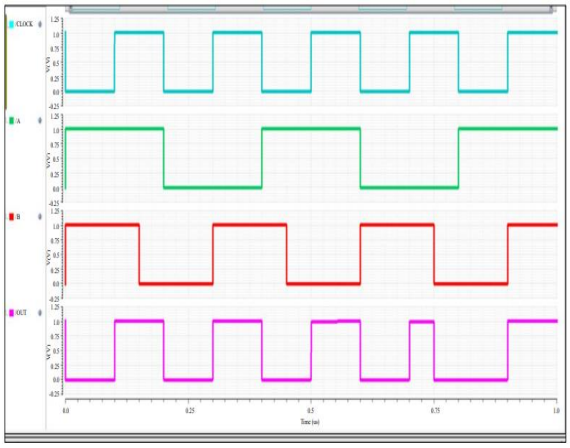

Figure 8: Transient analysis of Proposed domino logic based 2-input OR gate

The proposed circuit is compared with the existing domino circuits reported in [17], [19] and [20] in Table 1.

The proposed circuit uses 0.33nW and has propagation delay of 1.2 ps. Advantageously, the present circuit consumes at least 15% less power than the closest of the prior art circuits, and has a delay that is about 10% less than that of the closest of the prior art circuits. This improvement is due to a shorter leakage path, less keeper contention and a shorter effective evaluation path.

Table 1: Performance comparison of proposed circuit

Architecture	Power (nW)	Delay (ps)
LLKCDL [19]	0.63	7.3
HSSODL [20]	0.76	8.2
MHSCD [17]	0.95	9.3
HSCD [17]	0.83	8.7
CMFD [17]	1.10	10.2
HSCS [17]	0.56	7.1
SRLC [17]	0.53	6.9
Proposed	0.33	1.2

V. CONCLUSION

A low power and noise-tolerant domino logic architecture has been designed based on 7-nm FinFET technology. The footer and stacking devices ensure that the charge stored at the dynamic node is

not discharged due to leakage and also increases noise immunity, while the keeper transistor keeps the charge stored at the dynamic node. The semi-dynamic output stage has also been modified to eliminate unwanted precharge pulses from being transmitted to the output.

The simulation results validate that the proposed two-input OR gate has less power consumption, propagation delay. The design achieves 0.33 nW power consumption, 1.2 ps delay. Thus, the proposed architecture can be implemented for high speed, low-power and noise sensitive digital circuits in the advanced technology nodes of FinFET.

REFERENCES

[1] V. B. Sreenivasulu and V. Narendar, "Performance improvement of spacer engineered n-type SOI FinFET at 3-nm gate length," *AEU—International Journal of Electronics and Communications*, vol. 137, Art. no. 153803, 2021.

[2] Sharma and V. K. Sharma, "An efficient low power method for FinFET domino OR logic circuit," *Microprocessors and Microsystems*, vol. 95, Art. no. 104719, 2022.

[3] A. Razavieh, P. Zeitzoff, and E. J. Nowak, "Challenges and limitations of CMOS scaling for FinFET and beyond architectures," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 999–1004, 2019.

[4] V. B. Sreenivasulu and V. Narendar, "A comprehensive analysis of junctionless tri-gate FinFET towards low-power and high-frequency applications at 5-nm gate length," *Silicon*, vol. 14, pp. 2009–2021, 2021.

[5] V. K. Magraiya and T. K. Gupta, "ONOFIC pull-up approach in domino logic circuits using FinFET for subthreshold leakage reduction," *Circuits, Systems, and Signal Processing*, vol. 38, pp. 2564–2587, 2019.

[6] T. S. Kumar and S. L. Tripathi, "Leakage reduction in 18-nm FinFET-based 7T SRAM cell using self-controllable voltage-level technique," *Wireless Personal Communications*, vol. 116, pp. 1837–1847, 2020.

[7] S. V. K. Kajal, "FinFET: A beginning of non-planar transistor era," in *Nanoscale VLSI: Devices, Circuits and Applications*. Singapore: Springer, 2020, pp. 139–159.

[8] M. V. Nageswara Rao *et al.*, "Design and development of efficient SRAM cell based on FinFET for low-power memory applications," *Journal of Electrical and Computer Engineering*, 2023.

[9] M. Karamimanesh, E. Abiri, K. Hassanli, M. R. Salehi, and A. Darabi, "A robust and write-bit-line-free subthreshold 12T-SRAM for ultra-low-power applications in 14-nm FinFET technology," *Microelectronics Journal*, vol. 118, Art. no. 105185, 2021.

[10] J. V. Suman, K. K. Cheepurupalli, and H. L. Allasi, "Design of polymer-based trigate nanoscale FinFET for the implementation of a two-stage operational amplifier," *International Journal of Polymer Science*, vol. 2022, Art. no. 3963188, 2022.

[11] A. Tang, Y. Yang, C.-Y. Lee, and N. K. Jha, "McPAT-PVT: Delay and power modelling framework for FinFET processor architectures under PVT variations," *IEEE Transactions on Very Large-Scale Integration Systems*, vol. 23, pp. 1616–1627, 2015.

[12] S. Ilin, D. Ryzhova, and A. Korshunov, "Comparative analysis of standard-cell performance for 7-nm FinFET and 28-nm CMOS technologies considering parasitic elements," in *Proc. IEEE EIConRus*, 2018.

[13] K. Liao *et al.*, "Ultra-low power dissipation of improved complementary pass-transistor adiabatic logic circuits based on FinFETs," *Science China Information Sciences*, vol. 57, pp. 1–13, 2014.

[14] H. Mahmoodi-Meimand and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," *IEEE Transactions on Circuits and Systems I*, vol. 51, pp. 495–503, 2004.