Modeling of the Ferroelectric Field Effect Transistor

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***Abstract*—With an increase in the demand for microelectronics device there is also a thrust to explore novel device concepts like ferroelectric effects to overcome the limitation of CMOS based circuits. This has brought out to the fore the applications of Ferro-Electric FET (FEFET) which find huge potential in data computing along with global connectivity. However, the FEFET is besought with anomalies dealing with the threshold voltage arising on account of various factors. While few factors are inherently material property dependent, others are incorporated inadvertently due to the processes in fabrication. There is tremendous scope for the enhancement of performance parameters especially the variations of threshold voltage. This paper delves into the modeling of a FEFET, which requires the analysis from both perspectives i.e. the semiconductor along with the ferroelectric material. The Berkeley Short Chanel IGFET Model (BSIM)is used to evaluate various parameters for the semiconductor interface while the Preisach based modeling is used to elaborate upon the interstitial layer of the ferroelectric material. In exploring all these parameters several facets come to the fore, namely the material-based quantities which determine the polarization of the domains, and the operational terms like the applied voltage to enumerate the multi-domain polarization. Likewise, on the semiconductor part of the device the sub threshold leakage current, surface defects which inadvertently occur during fabrication process have to be accounted for in order to ensure that there is uniform distribution of the polarization domains in the ferroelectric material. Furthermore, it would also be interesting to note the behaviour of the device owing to the continuous drive to miniaturize the devices. Moreover, the effects which for now are apparently evaluated in 2 dimensions, could in the near future necessitate the validation using 3 dimensional equations.**

***Index Terms*—FEFET, BSIM, Preisach, subthreshold leakage, surface defects.**

I. INTRODUCTION

The Berkeley Short Chanel IGFET Model (BSIM) [1], [2] has been in use for long time to model transistors at micro/nanoelectronics dimensions. With an ever-increasing demand for high speed, low power and small size transistors there is also an enhancement in the interest to explore technologies beyond CMOS [3]. Moreover, with the hike in demand for applications being more sensitive to data retrieval and also long-term storage capacity, there is a renewed interest in developing ferroelectric based circuits [4].

Complementary MOSFETs, which offer a low-power dissipation for a high-speed circuit, are limited by the subthreshold swing (SS) [5] which cannot be scaled below 60 mV/dec. Hence, the Ferroelectric FET (FEFET) which works on the principle of negative capacitance [6], requires a modeling approach different as that used for MOSFET [7].

FEFET

This paragraph briefly describes the FEFET with the structural diagram in **Figure 1**, its equivalent circuit representation in **Figure 2** and the associated equations, thereafter.

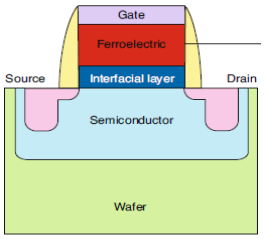

Figure 1: FEFET structure

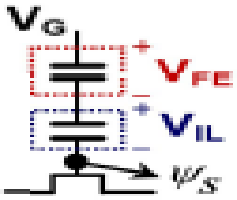

Figure 2: FEFET circuit equivalent

The Landau – Khalatnikov equation which describe the polarization of states of the FEFET is given by

$$E = \gamma_1 S^2 + \gamma_2 S^4 + \gamma_3 S^6 \quad (1)$$

Where E is the energy required for the particular domain formation and is represented by the dependence of polarization on the threshold voltage as

$$P_{FE}(V_{FE}) = m.F(V_{FE}) + b \quad (2)$$

BSIM Modeling for the Semiconductor interface

The above modeling is for the ferroelectric part of the FEFET, whereas the semiconductor part requires the BSIM based modeling, as shown in **Figure 3.**

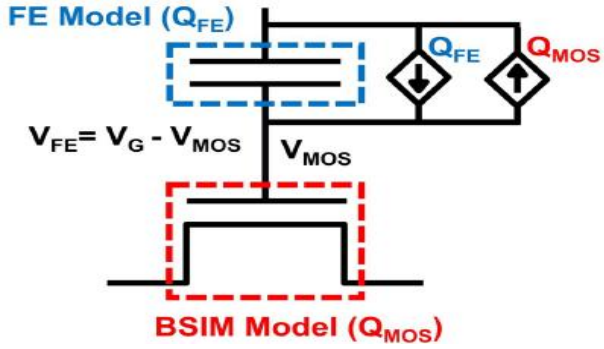

Figure 3: FEFET model

The polarization of the domains is dependent on the threshold voltage, which itself is a function of several material or operational parameters. These are specified using an internal node voltage V'_m as

$$V'_m = V_m + \Delta V \quad (3)$$

Where

$$. \Delta V = 0.5 * \Delta V_2 * \left(\frac{\Delta V_2}{\Delta V_1} - 1\right) \tan\left(\alpha(V_{FE} - b)\right) + \Delta V_2 * \left(\frac{\Delta V_1}{\Delta V_2} + 1\right) \quad (4)$$

Here, the charge of the ferroelectric layer and the semiconductor interface charge are shown separately as Q_{FE} *and* Q_{MOS}.

The BSIM-IMG when applied to a MOSFET involves the identification of the current in the 3 regions of operation namely cut-off, triode, and saturation regions. Effectively the formulation has to consider the individual regions of operation to ensure the continuity of the model from one switching operation to the next.

For a smooth transition from one region to another a parameter preprocessing has to be done by involving all the physical dimension terms like the channel length, and depletion width to the operational terms like back gate voltage, sub-threshold current etc.

However, in case of the FEFET sufficient precaution has to be taken, by means of accommodating the switching times of the polarization states as

$$V_{FE,hl} = -\frac{P_{FE}}{C_{FE}+C_{IS}} \quad (5)$$

Where $V_{FE,hl}$ is the polarization relaxation time or the time for high to low transition. The capacitance of the ferroelectric layer depends on the charge Q_{FE}, having the area and the thickness of the ferroelectric, as

$$Q_{FE} = \frac{\varepsilon_0 A_{FE}}{T_{FE}} V_{FE} + Q \quad (6)$$

The subthreshold swing then becomes a function of the gate and semiconductor dielectrics C_G *and* C_S as

$$\frac{\partial V_{FE}}{\partial V_s} = \left(1 + \frac{C_S}{C_G}\right) \quad (7)$$

II. CONCLUSION

It is evident that structural modifications are very much required to lead to an improvement in the performance parameters of the FEFET. Identical explorations could be on the anvil for further developments with memory specific requirements. For example, the use of FEFET or the Resistive-RAM i.e., RRAM could bolster the demand for non – volatile memories. This also entails that the mathematical formulation has to consider the necessary second order effects which otherwise tend to degrade the device performance.

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