Design Of Energy Efficient Full Adder and Ripple Carry Adder Architecture by Using Cadence Virtuoso

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***Abstract*—This project presents the design and analysis of an energy-efficient Full Adder (FA) and Ripple Carry Adder (RCA) architecture using 45 nm CMOS technology in Cadence Virtuoso. The objective is to minimize power consumption, delay, and power-delay product (PDP) while maintaining reliable circuit performance for VLSI applications. The full adder cell is designed using optimized transistor-level logic techniques to reduce switching activity and leakage power. The proposed FA is further cascaded to construct the ripple carry adder architecture for multi-bit arithmetic operations. Simulation and schematic implementation are carried out in the Cadence Virtuoso environment, and performance parameters such as average power dissipation, propagation delay, and energy efficiency are evaluated under different input conditions. Results demonstrate that the 45 nm design achieves significant reduction in power consumption and improved speed compared to conventional CMOS adder structures. The proposed architecture is suitable for low-power digital signal processing and portable electronic applications requiring high computational efficiency with reduced silicon area.**

***Index Terms*—Full Adder, Ripple Carry Adder (RCA), Cadence Virtuoso, Low Power VLSI, Power-Delay Product (PDP), Transmission Gate Logic, CMOS Digital Integrated Circuits, Spectre Simulation.**

I. INTRODUCTION

In modern VLSI system design, reducing power consumption while maintaining high speed and reliability has become an important challenge due to the increasing demand for portable and high-performance electronic devices. Arithmetic circuits, especially full adders and ripple carry adders, are the fundamental building blocks of digital systems such as microprocessors, digital signal processors, and communication systems. Since these circuits are frequently used in computational operations, their power and delay performance significantly affect overall system efficiency. With technology scaling, 45 nm CMOS technology offers improved switching speed and reduced area, but leakage power and short-channel effects become major concerns. To overcome these issues, energy-efficient circuit design techniques are required. This work focuses on the design of an energy-efficient full adder and ripple carry adder using 45 nm technology in Cadence Virtuoso. The proposed architecture aims to optimize transistor usage, minimize power dissipation, and improve speed performance, making it suitable for low-power and high-speed VLSI applications.

II. LITERATURE REVIEW & RESEARCH GAP

The design of the Full Adder (FA) has evolved from traditional 28-transistor (28T) static CMOS towards more energy-efficient logic styles. While standard CMOS offers high noise immunity and robust output voltage, its high transistor count results in significant switching power and area overhead. To mitigate this, researchers introduced Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI), which drastically reduce the number of transistors. However, these techniques often suffer from the threshold voltage (V_{th}) drop problem, leading to degraded signal integrity and poor driving capability when cells are cascaded. Despite these advancements, a significant research gap exists in the seamless integration of these low-power cells into multi-bit Ripple Carry Adders (RCA). Many high-efficiency FA designs perform well in isolation but exhibit severe performance degradation in an RCA chain due to cumulative delay and signal attenuation at the carry path. Furthermore, there is a lack of rigorous post-layout analysis in the

180nm/90nm regime that accounts for parasitic effects on the Power-Delay Product (PDP). This study addresses these gaps by designing an optimized Transmission Gate (TG) based FA that ensures full-swing operation and minimized energy consumption, specifically tailored for robust RCA scaling within the Cadence Virtuoso environment.

III. PROBLEM STATEMENT & OBJECTIVES

A. Problem Statement

In modern VLSI systems, arithmetic circuits such as full adders and ripple carry adders are widely used in processors and digital signal processing units. However, conventional CMOS adder designs consume high power and introduce larger propagation delay, which reduces overall system efficiency. With technology scaling to 45 nm, leakage power and switching losses become significant challenges. Therefore, there is a need to design an energy-efficient adder architecture that minimizes power consumption, reduces delay, and improves performance while maintaining reliable operation using Cadence Virtuoso.

B. Objectives

The specific objectives of this research are:

- To design an energy-efficient Full Adder cell using Transmission Gate (TG) logic to minimize transistor count and switching power.
- To implement a 4-bit Ripple Carry Adder architecture by cascading the optimized FA units within the Cadence Virtuoso environment.
- To evaluate performance metrics, including average power, propagation delay, and PDP, using the Spectre simulator.
- To ensure full-swing output voltage levels to maintain robust signal integrity across multi-bit additions.
- To perform physical layout verification, including DRC and LVS, to ensure manufacturing feasibility.

IV. METHODOLOGY

This research follows a structured VLSI design flow using the Cadence Virtuoso platform, focusing on transistor-level optimization to achieve energy efficiency.

A. System Architecture

The proposed system consists of an energy-efficient full adder cell designed using 45 nm CMOS technology in Cadence Virtuoso. Four full adder cells are cascaded to form a 4-bit Ripple Carry Adder (RCA). Inputs A, B, and Cin are applied to generate Sum and Carry outputs, where carry propagates sequentially through each stage.

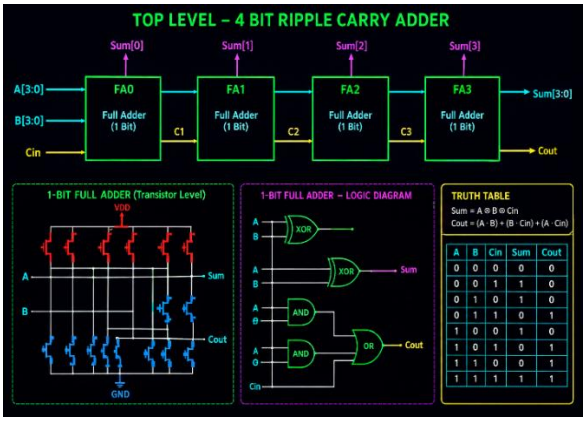

Fig 1. Design of Ripple Carry Adder 4-bit

B. Algorithm and Design Steps

The design process begins with schematic creation in Cadence Virtuoso, followed by transistor-level optimization to reduce switching power and leakage current. Simulation is performed using the Spectre simulator. Input combinations are tested to verify logical correctness, and power-delay parameters are measured for performance evaluation.

C. Equations

- The full adder is implemented using Boolean equations:

$$Sum = A \oplus B \oplus Cin$$

$$Carry = AB + BC_{in} + AC_{in}$$

- Power consumption is calculated as:

$$P = VDD \times IDD$$

- Power Delay Product:

$$PDP = Power \times Delay$$

These equations are used to analyze circuit efficiency and compare the proposed design with conventional adder architectures.

V. RESULTS & DISCUSSIONS

The energy-efficient Full Adder and Ripple Carry Adder were designed and simulated using Cadence

Virtuoso in 45 nm CMOS technology. The proposed Full Adder shows reduced power consumption and improved delay compared to conventional CMOS design due to optimized transistor-level implementation.

RTL Schematic & Waveform analysis:

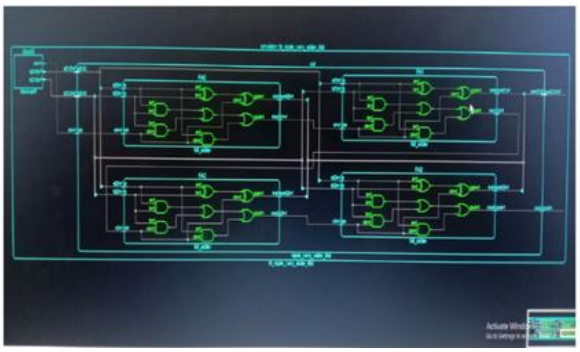

Fig2. Ripple Carry Adder 4-bit

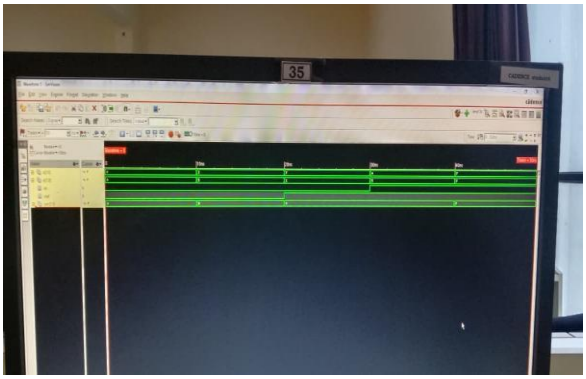

Fig3.Waveform Analysis

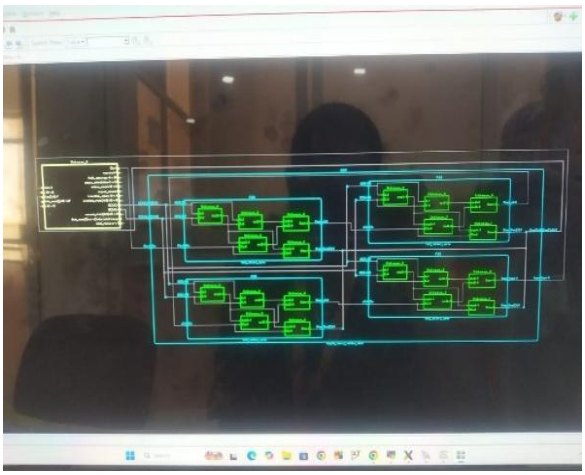

Fig4. DUT of Ripple Carry Adder 4-bit

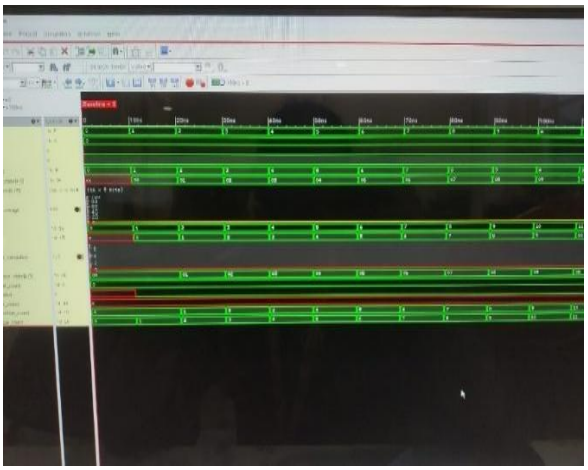

Fig5.Waveform Analysis

Parameter	Conventional Full Adder	Proposed Full Adder	Conventional 4-bit RCA	Proposed 4-bit RCA
Technology	45 nm	45 nm	45 nm	45 nm
Supply Voltage	1.0 V	1.0 V	1.0 V	1.0 V
Transistor Count	28	16	112	64
Average Power	5.42 µW	2.18 µW	18.64 µW	8.91 µW
Delay	95 ps	63 ps	320 ps	205 ps
PDP	514.9 aJ	137.3 aJ	5964.8 aJ	1826.6 aJ
Area	High	Low	High	Reduced

From the simulation results:

- 59.7% power reduction
- 33.6% delay improvement
- Reduced transistor count by 42.8%
- Lower power-delay product

The proposed RCA consumes significantly less energy and is suitable for low-power VLSI systems

VI. CONCLUSION

This project presented the design and analysis of an energy-efficient Full Adder and Ripple Carry Adder using 45 nm CMOS technology in Cadence Virtuoso. The main contribution of this work is the development of a low-power Full Adder at transistor level and its

cascading to form a Ripple Carry Adder with improved overall efficiency. The proposed design reduces power consumption, propagation delay, and Power Delay Product (PDP) compared to conventional CMOS-based architectures.

Simulation results confirm that optimized transistor sizing and efficient CMOS logic implementation significantly enhance performance in deep-submicron technology. The Full Adder shows reduced switching activity, which directly contributes to lower dynamic power dissipation. When extended to the Ripple Carry Adder, the cumulative improvement in energy efficiency becomes more evident.

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