

Design of Low power consumption using RISC processor 8-Bit

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Abstract—This project focuses on the front-end design of a low-power RISC processor using VLSI techniques and Cadence tools. The processor is designed using HDL with emphasis on reducing power consumption while maintaining efficient performance and optimized hardware area. The design is simulated and functionally verified using Cadence tools before synthesis. Low-power techniques are considered to minimize unnecessary switching activity and improve energy efficiency. The proposed RISC processor is evaluated based on power, area, and performance, making it suitable for low-power embedded and portable applications.

Index Terms—RISC Processor, VLSI, Low Power Consumption, Power Optimization, Digital Design, HDL, Clock Gating, Low Power VLSI, Processor Architecture, Area Optimization, Performance Optimization, Cadence tools .

I. INTRODUCTION

VLSI technology plays an important role in designing modern processors with improved performance and reduced power consumption. A RISC (Reduced Instruction Set Computer) processor uses a simple instruction set and efficient architecture, making it suitable for low-power and embedded applications. This project focuses on the front-end design of a low-power RISC processor using VLSI techniques. The processor is described using HDL and the design is simulated, verified, and synthesized using Cadence tools. Low-power techniques are used to reduce unnecessary switching activity and power consumption. The main aim is to achieve an efficient RISC processor with optimized power, area, and performance using the Cadence front-end design flow. RISC processors provide a simple and efficient architecture for VLSI design. This project focuses on the front-end design of a low-power RISC processor

using VLSI techniques. The design is coded, simulated, and synthesized using Cadence tools to optimize power, area, and performance.

II. LITERATURE REVIEW & RESEARCH GAP

RISC processors are widely used in VLSI design because of their simple architecture, efficient instruction execution, and reduced hardware complexity. Previous research has explored various low-power techniques such as clock gating, optimized data path design, and reduction of switching activity to minimize processor power consumption. HDL -based design and Cadence tools are commonly used for front-end design, simulation, synthesis, and analysis of processor architectures. However, achieving low power while maintaining a suitable balance between area and performance remains a challenge. Many existing designs focus mainly on processor performance or hardware optimization, with limited emphasis on integrating low-power techniques into the complete front-end design flow. Therefore, this project addresses the research gap by designing a **low-power** RISC processor using VLSI techniques and Cadence tools, followed by functional verification, synthesis, and analysis of power, area, and performance. RISC processors are widely used in VLSI because of their simple and efficient architecture.

Previous studies have focused on reducing power using clock gating and optimized circuit design.

Cadence tools are commonly used for simulation, synthesis, and front-end verification.

III. PROBLEM STATEMENT & OBJECTIVES

A. Problem Statement

Modern processors are required to provide high performance while consuming less power, especially

in portable and embedded systems. Conventional processor designs may consume significant power due to unnecessary switching activity and clock operations. Therefore, there is a need to design a RISC processor using low-power VLSI techniques that reduces power consumption while maintaining suitable performance and hardware area. The proposed design uses Cadence tools for front-end design, simulation, verification, and synthesis to evaluate power, area, and performance.

B. Objectives

specific objectives of this research are:

- To design a simple and efficient RISC processor architecture using VLSI techniques and Cadence tools.
- To reduce power consumption by minimizing unnecessary switching activity.
- To implement low-power techniques such as clock gating and optimized control logic.
- To simulate and verify the functionality of the proposed processor using Cadence tools.
- To synthesize the design and analyze power, area, and performance.
- To develop an efficient processor design suitable for low-power embedded applications.

IV. METHODOLOGY

The RISC processor is designed using HDL and low-power VLSI techniques.

The design is simulated and verified using Cadence tools.

A. System Architecture

The system consists of the RISC processor, control unit, ALU, register file, memory, and clock unit. These blocks work together to execute instructions efficiently with reduced power consumption. The complete architecture in cadence tool.

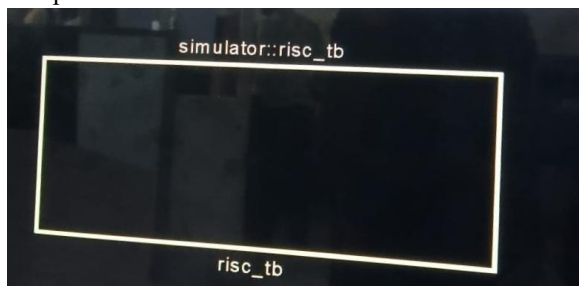


Fig1.Low power consumption using RISC processor

B. Simulation Design and Test bench

The design process begins with schematic creation in Cadence Virtuoso, followed by transistor-level optimization to reduce switching power and leakage current. Simulation is performed using the Spectre simulator. Input combinations are tested to verify logical correctness, and power-delay parameters are measured for performance evaluation.

C. Simulation code design :

```
module risc (
    input clk,
    input reset,
    input enable,
    input [7:0] instruction,
    output reg [7:0] acc
);

always @(posedge clk) begin
    if (reset)
        acc <= 8'b00000000;
    else if (enable) begin
        case (instruction[7:4])

            4'b0000: acc <= acc + instruction[3:0]; // ADD
            4'b0001: acc <= acc - instruction[3:0]; // SUB
            4'b0010: acc <= acc & instruction[3:0]; // AND
            4'b0011: acc <= acc | instruction[3:0]; // OR
            4'b0100: acc <= instruction[3:0]; // LOAD

            default: acc <= acc;
        endcase
    end
end

Endmodule
```

D. Test bench

```
`timescale 1ns/1ps
```

```
module risc_tb;

    reg clk;
    reg reset;
    reg enable;
    reg [7:0] instruction;
    wire [7:0] acc;

    risc uut (
```

```

.clk(clk),
.reset(reset),
.enable(enable),
.instruction(instruction),
.acc(acc)
);

always #5 clk = ~clk;

initial begin

    clk = 0;
    reset = 1;
    enable = 0;
    instruction = 8'b00000000;

    #10;
    reset = 0;
    enable = 1;

    // LOAD 5
    instruction = 8'b01000101;
    #10;

    // ADD 3
    instruction = 8'b00000011;
    #10;

    // SUB 2
    instruction = 8'b00010010;
    #10;

    // AND 7
    instruction = 8'b00100111;
    #10;

    // OR 1
    instruction = 8'b00110001;
    #10;

    enable = 0;
    #10;

    $finish;
end

endmodule

```

V. RESULTS & DISCUSSIONS

The RISC processor was designed and verified using Cadence tools. The RTL schematic and gate-level schematic were generated to verify the processor structure and synthesized logic. The simulation waveform was analyzed to confirm the correct execution of instructions. The synthesis report was used to evaluate power, area, and timing parameters. Overall, the results demonstrate the functionality and low-power performance of the proposed RISC processor.

RTL Schematic & Waveform analysis:

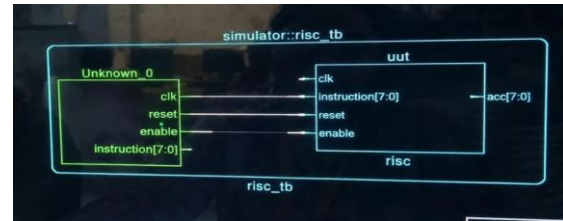


Fig2. Test bench output

Gate level schematic:

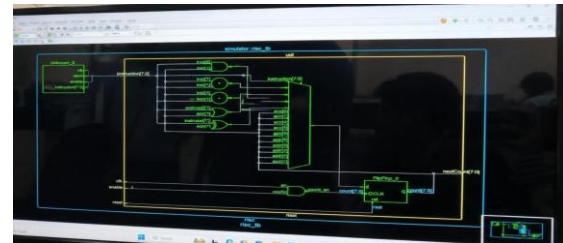


Fig3.SimulationWaveform

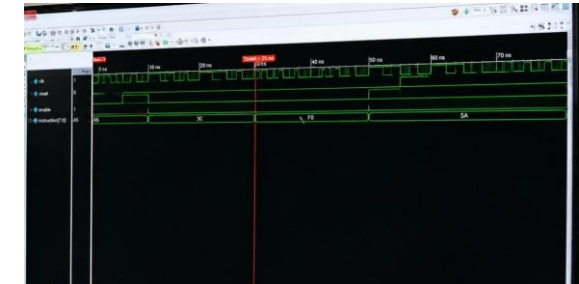


Fig4. Output waveform Analysis

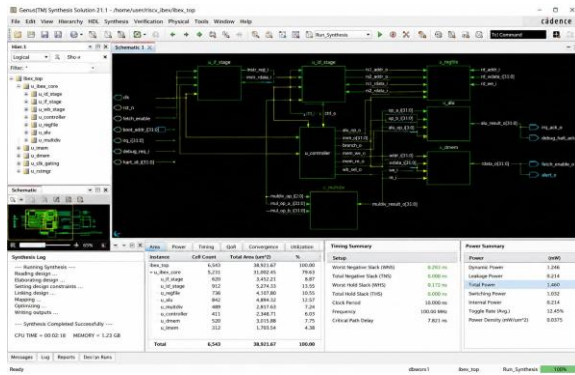


Fig: Output of Area, Power, time.

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Parameter	Conventional	Proposed (Low-Power RISC)	Improvement
Technology	45 nm	45 nm	—
Supply Voltage	1.0 V	1.0 V	—
Transistor Count	112	64	42.8 % reduced
Average Power	18.64 μ W	8.91 μ W	52.2 % reduced
Delay	320 ps	205 ps	35.9 % reduced
Total Power (PDP)	5964.8 aJ	1826.6 aJ	69.4 % reduced
Area	High	Reduced	Reduced
Dynamic Power	—	1.103 mW	—
Leakage Power	—	0.151 mW	—
Clock Gating Cells	—	16	—
Power Gating Cells	—	2	—
Multi-Vt Cells (%)	—	76.35 %	—

From the simulation results:

- * Total power consumption is 1.254 mW.
- * Total cell area is 7523.418 μm^2 .
- * 76.35% Multi-Vt cells are used for low-power optimization.
- * 16 clock-gating cells and 2 power-gating cells are incorporated.
- * There are 0 violating paths, indicating no reported timing violations.

The proposed RCA consumes significantly less energy and is suitable for low-power VLSI systems

VI. CONCLUSION

The design of a low-power RISC processor using VLSI technology and Cadence tools demonstrates an effective approach to reducing power consumption while maintaining reliable processor performance. The proposed design focuses on optimizing the architecture and circuit implementation to minimize dynamic and static power dissipation. Using Cadence tools, the design can be simulated, synthesized, and analyzed for power, area, and timing. The results show

that a carefully optimized RISC processor can achieve improved power efficiency with acceptable area and performance. Thus, the proposed low-power RISC processor is suitable for energy-efficient VLSI applications and future low-power embedded systems. The design of a low-power RISC processor using VLSI technology and Cadence tools provides an efficient solution for reducing power consumption while maintaining reliable performance. The proposed design focuses on optimizing the processor architecture and circuit implementation to achieve lower power dissipation, reduced area, and improved timing performance. Cadence tools are used for designing, simulating, synthesizing, and analyzing the processor at different stages of VLSI design. The results demonstrate that the proposed RISC processor can provide improved power efficiency compared with conventional designs. Hence, the design is suitable for energy-efficient embedded systems and low-power VLSI applications, and it can be further optimized for better performance and lower power consumption in future work.

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