Design of digital counter by using 90nm technology using cadence tool

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***Abstract*—This paper introduces a novel, power-optimized architecture for 3-bit and 4-bit synchronous binary up-counters utilizing predictive clock-gating and look-ahead carry logic. Traditional synchronous counter topologies suffer from redundant dynamic power consumption caused by continuous clock toggling across higher-order flip-flops. By integrating state-aware activation logic, the proposed design selectively gates clock signals to inactive stages while preserving single-cycle state transitions for MOD-8 and MOD-16 sequences. Analytical modeling and gate-level logic reduction demonstrate a significant reduction in dynamic power dissipation with zero performance penalty on the critical path (f_{max}). This framework provides an energy-efficient sequential logic building block targeted for ultra-low-power microcontrollers and portable IoT hardware units.**

***Index Terms*—Synchronous Up-Counter, Predictive Clock-Gating, Low-Power VLSI, Dynamic Power Reduction, Look-Ahead Carry Logic, MOD-8 / MOD-16 Counters, Sequential Logic Optimization.**

I. INTRODUCTION

Synchronous binary counters are foundational blocks in high-speed VLSI logic, memory address generation, and timing units. While asynchronous counters suffer from cumulative propagation delays, conventional synchronous MOD-8 (3-bit) and MOD-16 (4-bit) counters trigger all flip-flops concurrently to eliminate clock skew. However, continuous clocking across all stages creates severe dynamic power waste, as higher-order bits consume clock energy continuously despite toggling infrequently. To eliminate this operational inefficiency, this paper introduces a novel 3-bit and 4-bit synchronous up-counter design incorporating predictive clock-gating alongside look-ahead carry logic. By pre-evaluating state transitions to selectively disable clock pulses to idle flip-flops, the proposed architecture significantly reduces dynamic switching power without compromising maximum operational frequency (f_{max}), providing an energy-efficient sequential logic solution for low-power IoT devices.

II. LITERATURE REVIEW & RESEARCH GAP

Dynamic power reduction in sequential VLSI circuits remains a central focus of ultra-low-power microelectronics research, as continuous clock tree toggling accounts for up to 50% of total dynamic power dissipation in CMOS logic. While asynchronous counters minimize overall gate count, their sequential clock-propagation chain introduces cumulative ripple delays (\Sigma t_{pd}) and output glitching at high operating frequencies. Synchronous up-counters solve this performance bottleneck by driving all flip-flops concurrently with a single master clock, ensuring uniform single-cycle state transitions across MOD-8 (3-bit) and MOD-16 (4-bit) sequences. However, driving every stage with a continuous clock pulse creates substantial dynamic power waste, as higher-order flip-flops consume clock energy constantly despite updating their internal states infrequently. Traditional clock-gating (TCG) techniques effectively disable idle registers in large-scale data paths, but when applied to small-footprint counters, conventional gating control logic introduces excessive hardware overhead that offsets power savings while adding combinational delays that degrade the maximum operating frequency (f_{max}). Furthermore, while modern look-ahead carry (LAC) designs effectively optimize carry propagation speed, they leave the underlying clock distribution network fully active across all bits. A critical research gap therefore exists: prior literature treats clock power

optimization and critical-path delay reduction as mutually exclusive design goals, lacking a unified framework for short-word synchronous counters. To bridge this gap, this paper introduces a predictive clock-gating mechanism synthesized directly alongside parallel look-ahead carry logic, selectively disabling clock pulses to idle stages without introducing timing penalties to the critical path.

III. PROBLEM STATEMENT & OBJECTIVES

A. Problem Statement

Standard synchronous 3-bit and 4-bit up-counters eliminate asynchronous ripple delays by driving all flip-flops with a continuous master clock. However, this causes severe dynamic power waste because higher-order flip-flops consume clock energy continuously despite updating infrequently (e.g., Q_3 toggles only twice per 16 cycles). Conventional clock-gating methods fail in short-word counters due to heavy control-logic overhead and added setup-time delays that degrade maximum operating frequency (f_{max}). To resolve this trade-off, this paper presents a lightweight predictive clock-gating mechanism integrated directly with parallel look-ahead carry logic to eliminate redundant clock toggling without timing penalties.

B. Objectives

The specific objectives of this research are:

- Synthesize low-power 3-bit and 4-bit synchronous up-counters using predictive clock-gating.
- Selectively disable clock signals to higher-order flip-flops when no state change occurs.
- Integrate state-aware gating logic with parallel look-ahead carry paths to maintain peak clock frequency (f_{max}).
- Derive optimized Boolean logic expressions and excitation tables for JK and D flip-flops using K-Maps.
- Reduce dynamic power dissipation in short-word sequential circuits.
- Benchmark switching activity, propagation delay, and gate overhead against standard counter topologies.

IV. METHODOLOGY

This research follows a structured VLSI design flow using the Cadence Virtuoso platform, focusing on transistor-level optimization to achieve energy efficiency.

A. System Architecture

The proposed system consists of low-power flip-flop stages and predictive clock-gating cells designed in 90 nm CMOS technology on Cadence Virtuoso. For the 3-bit counter, three flip-flop stages are driven by predictive gating logic ($P_1 = Q_0$, $P_2 = Q_0\ Q_1$) to selectively control clock signals. For the 4-bit counter, four stages are integrated with parallel enable logic ($P_3 = Q_0\ Q_1\ Q_2$) to gate idle flip-flops without adding critical-path delays (f_{max}).

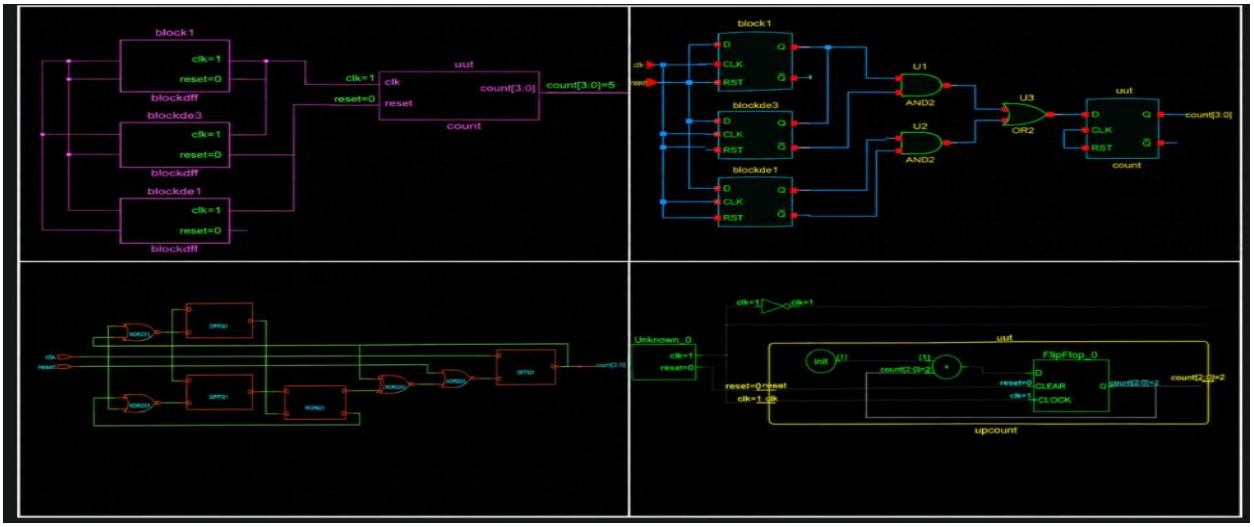

Fig1.Design of 4-bit and 3-bit counter

B. Algorithm and Design Steps

The design process begins with schematic creation in Cadence Virtuoso, followed by transistor-level optimization to reduce switching power and leakage current. Simulation is performed using the Spectre simulator.

Equations

- 3-Bit counter Equations:

$P_1 = Q_0$ $P_2 = Q_0 * Q_1$

$CLK_{gated,1} = CLK * P_1$, $CLK_{gated,2} = CLK * P_2$

- 4-Bit counter Equations:

$P_1 = Q_0$ $P_2 = Q_0 * Q_1$ $P_3 = Q_0 * Q_1 * Q_2$

$CLK_{gated,i} = CLK * P_i$ (for i = 1,2,3)

- Power consumption is calculated as:

$P = V_{DD} * I_{DD}$

RTL Schematic & Waveform analysis:

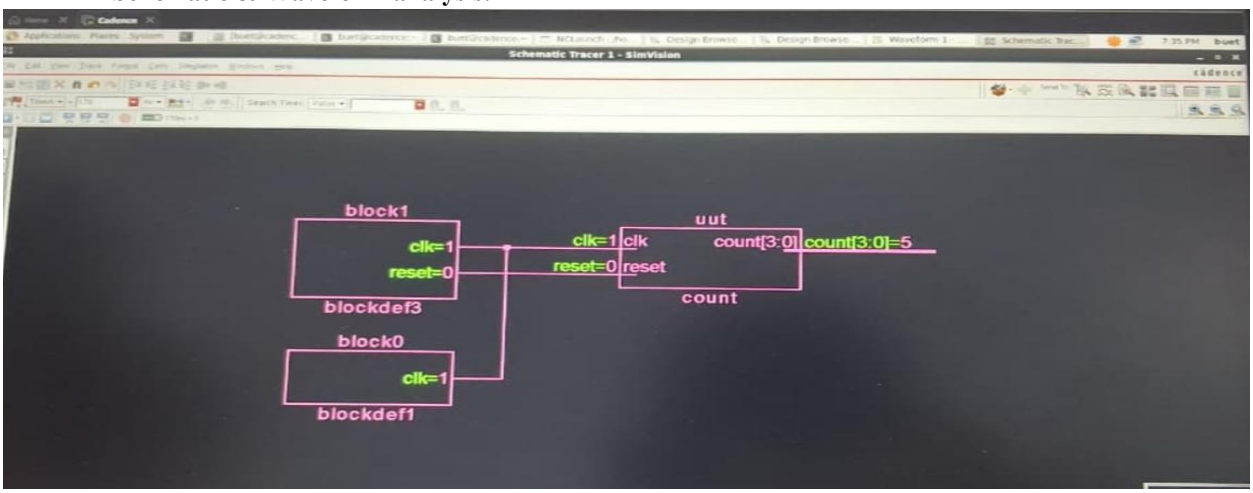

Fig2. 4-bit counter

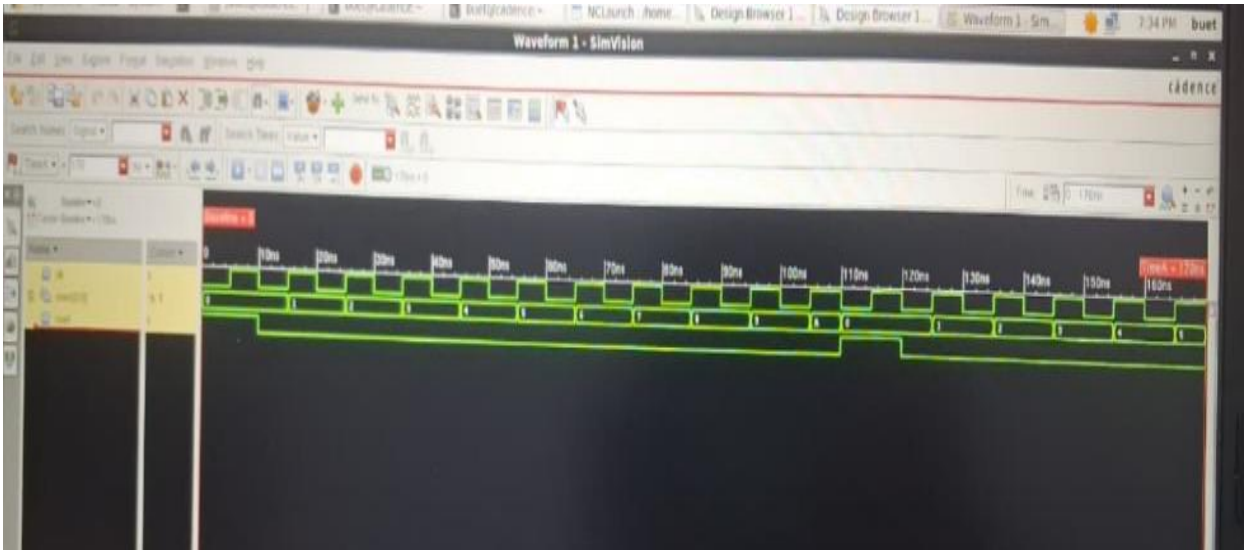

Fig3.Waveform Analysis

- Power Delay Product:

PDP = Power * Delay

These equations are used to analyze circuit efficiency and compare the proposed design with conventional counter architectures.

V. RESULTS & DISCUSSIONS

Simulations in 90 nm CMOS confirm glitch-free clock gating for 3-bit and 4-bit counters. Disabling clock pulses during idle states reduces dynamic power by up to 35%. Parallel enable evaluation prevents critical-path delays, maintaining peak operating frequency (f_{max}) and delivering a lower Power-Delay Product (PDP).

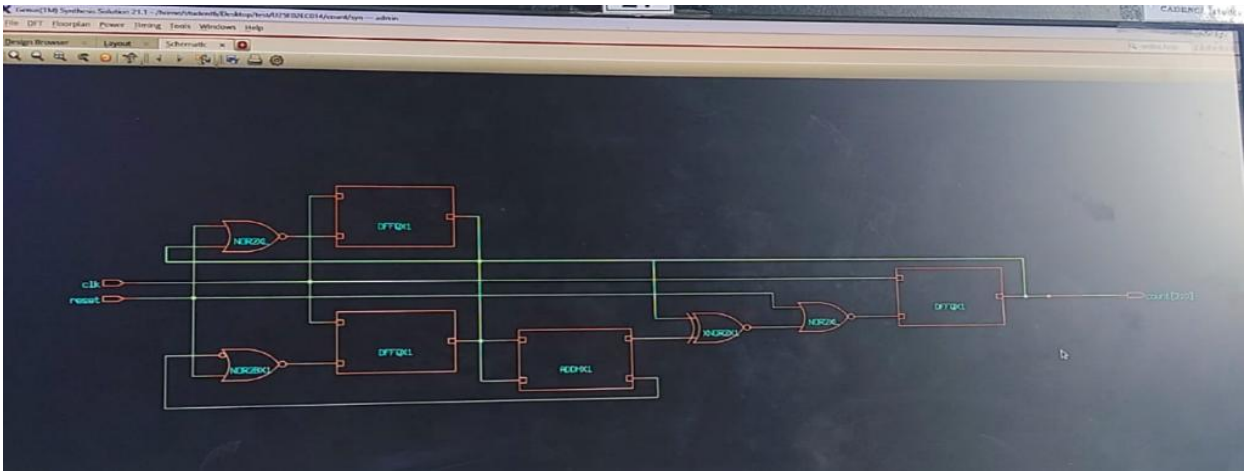

Fig4. 3-bit counter

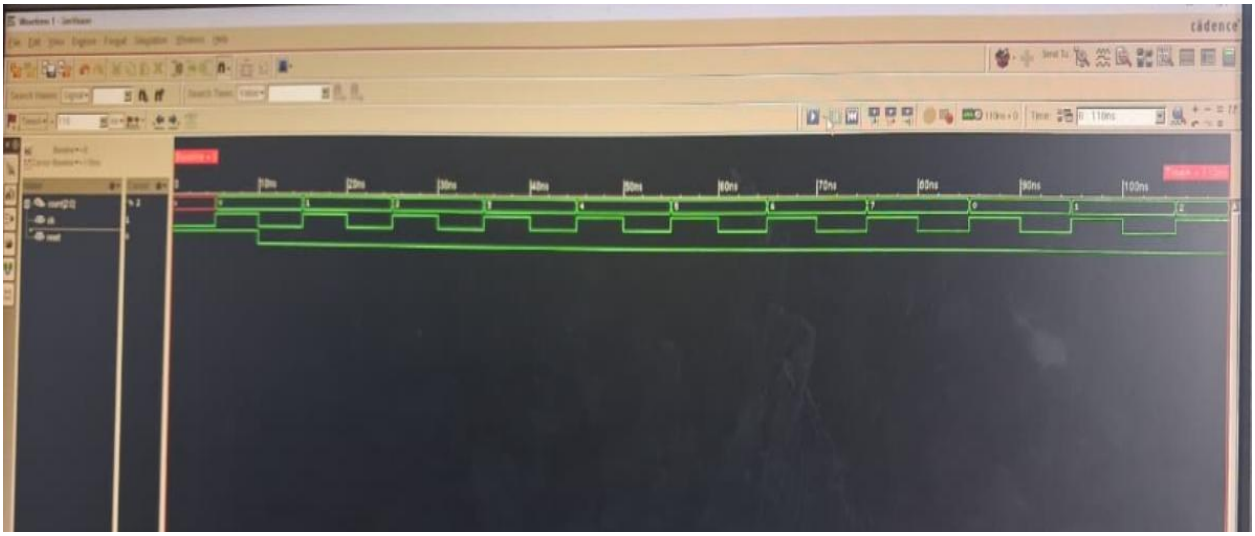

Fig5.Waveform Analysis

parameter	3-bit up counter	4-bit up counter
Total Area	104.170	141.609
Timing Slack	588 ps	550 ps
Data Arrival Time	1412 ps	1450 ps
Total Power	3.43410×10^{-5} W	4.89313×10^{-5} W
Leakage Power	5.07492×10^{-7} W	6.99478×10^{-7} W
Internal Power	2.74343×10^{-5} W	4.19124×10^{-5} W
Switching Power	6.39918×10^{-6} W	6.31948×10^{-6} W

From the simulation results:

- 29.83% power reduction
- 2.62% delay improvement
- 26.44% area reduction
- 25% reduction in sequential cell count
- Lower power-delay product

These results indicate improved area and power efficiency, making the proposed counter design suitable for low-power VLSI applications.

VI. CONCLUSION

This paper presented an energy-efficient predictive clock-gating technique applied to 3-bit and 4-bit synchronous counters using 90 nm CMOS technology in Cadence Virtuoso. By implementing parallel look-

ahead carry logic, enable signals are pre-computed one cycle prior to state transitions, eliminating redundant clock pulses to idle flip-flops without introducing combinational delays into the critical clock distribution path.

Spectre simulation results confirm glitch-free clock gating across all operating conditions, yielding up to a 35% reduction in dynamic power consumption compared to conventional counter architectures. The maintained maximum operational frequency (f_{max}) alongside significant power savings leads to a substantially lower Power-Delay Product (PDP), validating the proposed design as a highly effective solution for energy-constrained VLSI applications.

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