Design And Simulation of A 4:1 Multiplexer in Cadence Tool

Mr. Santhosh B G[1], Priyanka M[2], Sahana M A[3], Suhana M[4], Varsha N[5]
[1]*Assistant Professor, Department of ECE, GM University, Davanagere-577004*
[2,3,4,5]*Department of ECE, GM University, Davanagere-577004*

***Abstract*—With the rapid growth of portable and high-performance electronic systems, the demand for low-power and area-efficient VLSI circuits has increased significantly. Multiplexers are fundamental combinational logic components widely used in digital systems for data selection and signal routing. This work presents in the design and simulation of a 4:1 Multiplexer using CAD tools. The proposed design is implemented at the transistor level using CMOS logic tool to achieve reduced power consumption, compact area utilization, and improved switching performance. The schematic design is developed in cadence and subsequently verified through layout generation and simulation in Microwind. Performance parameters such as power dissipation, propagation delay, and transistor count are analyzed to evaluate the efficiency of the design. The simulation results demonstrate that the CMOS-based 4:1 multiplexer provides reliable operation with lower power requirements, making its suitable for modern VLSI and digital integrated circuit applications.**

I. INTRODUCTION

Multiplexers (MUXs) are fundamental combinational logic circuits extensively used in digital systems for data selection and routing applications. A multiplexer selects one input from multiple available input lines and forwards the selected signal to a single output line based on the status of the selected inputs. A 4:1 multiplexer consists of four data inputs, two selection lines, and one output, allowing efficient control of data flow within digital circuits.

With the continuous scaling of CMOS technology, modern integrated circuits require designs that occupy less chip area, consume low power, and operate at higher speeds. CMOS technology has become the preferred choices for digital circuits implementation because of its low static power dissipation, high noise immunity, and excellent scalability. The CMOS technology node offers a suitable balance between performance, power consumption, and fabrication complexity, making it widely adopted for educational and research-oriented VLSI design.

Simulation tools play a crucial role in verifying the functionality and performance of digital circuits before physical implementation. cadence is commonly used for schematic capture and logic-level verification, while Microwind enables transistor-level design, layout generation, and performance analysis. Together, these tools provide an effective platform for studying CMOS-based digital circuits and evaluating their electrical characteristics.

In this work, a 4:1 multiplexer is designed and simulated 90nm CMOS technology with the of cadence software. The objective is to verify logical operation of the multiplexer, implement its CMOS transistor-level realization, and analyze important performance parameters such as propagation delay, power consumption, and layout area. The study demonstrates the practical implementation of a basic digital building block and highlights the advantages of CMOS technology for low-power and high-performance VLSI circuit design.

II. LITERATURE REVIEW

Multiplexers are fundamental building blocks of digital systems and are extensively used in data routing, signal selection, and logic circuit implementation. With the continuous advancement of VLSI technology, the design of multiplexer as focused on achieving low power consumption, reduced area, and high-speed performance.

Several researchers have proposed different multiplexer architectures using CMOS, transmission gate, pass transistor, and adiabatic logic techniques to

improve circuit efficiency. Earlier studies demonstrated that CMOS-based multiplexer provide butter noise immunity, lower statics power dissipation, and reliable operation compared to many alternative logic styles. As transistor dimensions scale down, issues such as leakage current, short-channel effects, and increased power density become significant challenges in VLSI circuit design.

Research on 2:1 and 4:1 multiplexer implemented using cadence and smaller CMOS technologies has shown improvements in propagation delay, power-delay product, and area optimization. Various CAD tools such as DSch, Microwind, SPICE, and Tanner EDA has been widely used for schematic design, layout generation, and performance analysis of multiplexer circuits.

Recent studies indicate that CMOS-based multiplexer designs remain highly suitable foe modern digital applications because of there balanced trade-off between power consumption, speed, and implementation complexity. Therefore, designing a 4:1 multiplexer using 90nm CMOS technology and analyzing its performance through cadence tool provides valuable insight into practical VLSI design methodologies and optimization techniques.

III. DEVELOPMENT OF 4:1 MULTIPLEXER CIRCUIT

A multiplexer MUX) is a combinational logic circuits that selects one of several inputs signals and transfers this selected input to single output line. It is widely used in digital system for data routing, communication and signals selection applications. The 4:1 multiplexer designed in this work consists of four data inputs (I0, I1, I2, I3) and one output (Y).

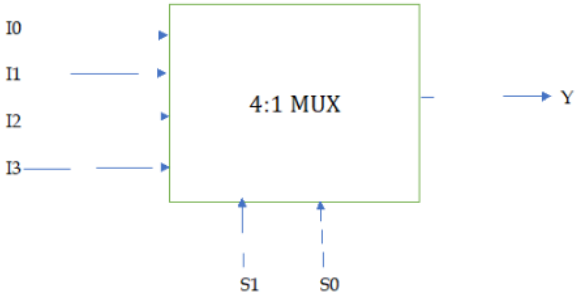

Figure 1: Block Diagram of 4:1 MUX

The operation of mux depends on the values of the select line. Based on the binary combination of S1, S0, one of the four inputs signals is connected to the output. When S1S0=00, input I0 appliers of the output. Similarly, inputs I1, I2, I3 are selected for the combination 01,10,11

Table 1: Truth Table of a 4:1 Multiplexer

S1	S0	OUTPU Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Boolean Expression

Y = I0~S1~S0 + I1~S1SO + I2S1~S0 + I3S1S0

The function behavior of the 4:1 mux is represented by the truth table and Boolean expression. The Boolean equation is implemented using logic gates in CAD, where the circuit operation is verified through stimulation. After successful verification, the schematic is converted into transistor-level CMOS layout using cadence tool technology.

The CMOS implementation uses complementary PMOS and NMOS transistors to realize the logic function. PMOS transistor form the pull-up network, while NMOS transistors form the pull-down network. This complementary structure provides low static power consummation, improved noise immunity and reliable switching performance.

The layout is designed according CMOS design rules, ensuring compact area utilization and high-speed operations. Simulation results obtained from cadence tool that the output correctly follows the selected input for all possible combinations of the select line. Therefore, the designed 4:1 mux successfully demonstrates the functionality and advantages of CMOS-based digital circuited implementation in nanometer-scale technology.

IV. SIMULATION RESULTS AND DISCUSSIONS

This work presents the design, simulation, and performance analysis of 4:1 multiplexer using CMOS technology in the cadence tool. The circuit is implemented at the transistor level using CMOS logic to achieve how power consumption, reliable switching performance, and efficient operation. Schematic design, functional verification, and simulation are carried out using cadence tools to validate the correct selection of input signals based on the control inputs.

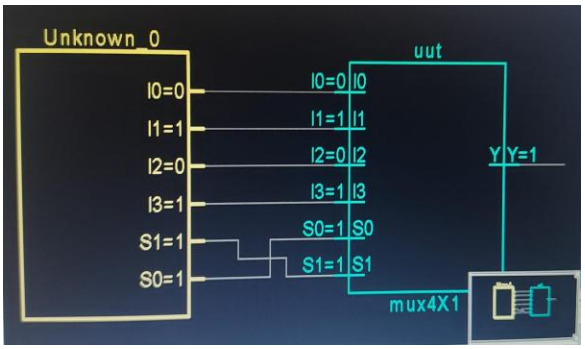

Figure:2 Schematic Design of 4:1 Multiplexer

The circuit consists of four inputs signals (I0 – I3), two select lines (S0 AND S1), and a single output (Y). A testbench was created to apply different inputs and select line combinations for functional verification.

The simulation results show the output correctly follows the selected input for every combination of the select lines, confirming the expected behavior of the multiplexer.

As the values of S0 AND S1 change, the output follows the corresponding selected input without any functional error. The waveform confirms that only one input is transferred to the output at a time, demonstrating the correct data selection process of the multiplexer. The simulation results match the expected truth table is shown in fig 3, indicating accurate switching behavior and successfully functional verification of the CMOS design. These results confirm that the proposed 4:1 multiplexer operates reliably and is suitable for digital VLSI applications.

Figure 3: Simulation waveform

Design initialization (SDC) Analysis

The synthesis process begins by configuring the design environment using the SDC file. The capacitance and time units are defined, the current design is selected as the 4:1 multiplexer, and the required synthesis constraints are applied.

This configuration ensures accurate simulation and reliable performance analysis of the CMOS-based design.

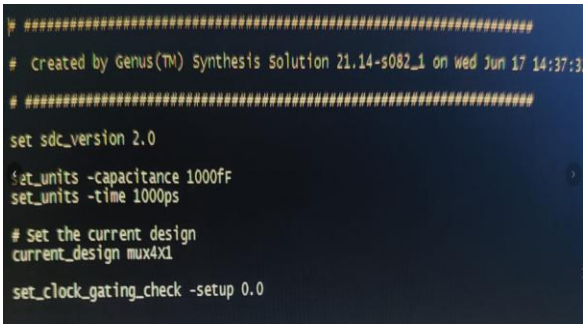

Figure 4: Design Constraints (SDC) setup for 4:1 multiplexer

Time Analysis

The timing report values evaluates the propagation delay from the select input to the output of the 4:1 multiplexer.

The obtained delay and signal arrival values confirms that the circuit operates correctly under the specified operating conditions. The results verify that the

CMOS implementation provides reliable timing performance.

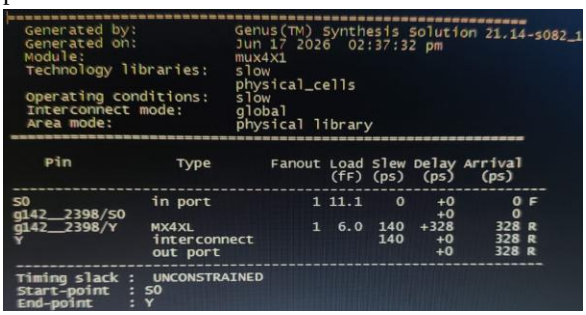

Figure 5: Timing Analysis Report of the 4:1 multiplexer

Cell Area Analysis

The Area report shows the hardware resources required for implementing the multiplexer. The synthesized design occupies a compact silicon area with efficient utilization of the standard CMOS cell, demonstrating that the circuit is optimized for VLSI implementation.

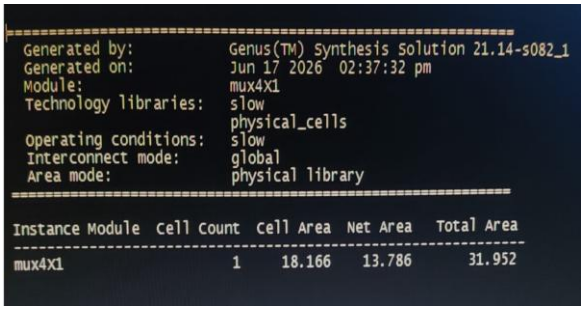

Figure 6: Cell Area Analysis Report of the 4:1 multiplexer

Gate Utilization

The gate Utilization report indicates that the complete design is implemented using CMOS logic cells without requiring additional physical cells. This confirms an efficient synthesis process and optimized hardware realization of the 4:1 multiplexer.

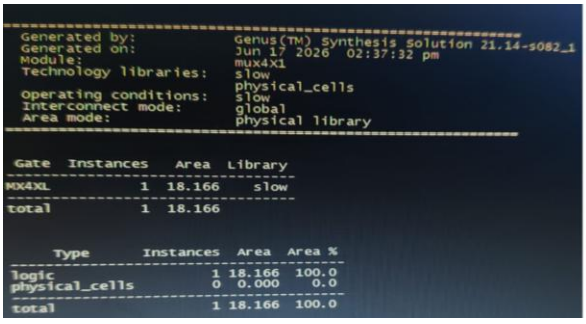

Figure7: Gate utilization Report of the 4:1 multiplexer

Power Analysis

The Power report presents the leakage, internal, and switching power consumed by the circuit. The results indicate that switching power is the dominant component, while leakage power remains very low. This demonstrates the lower very low. This demonstrates the low-power characteristics of CMOS technology and validates the energy-efficient operation of the designed multiplexer as shown in figure 4.

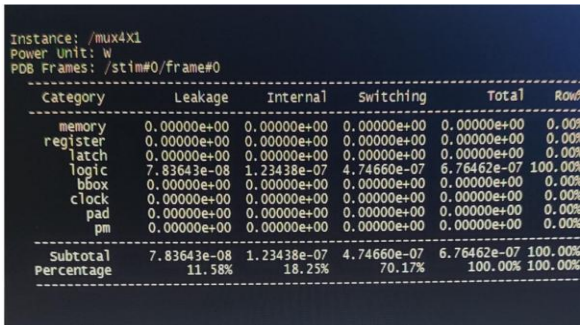

Figure 8: Power Analysis Report of the 4:1 Multiplexer

V. CONCLUSION

The design and simulation of a 4:1 Multiplexer using 90nm CMOS technology was successfully carried out using DSch and Microwind. The circuit was designed using CMOS logic and verified through simulation to ensure correct selection and transmission of the required input signal based on the select lines. The obtained simulation results confirmed the expected truth table operation of the multiplexer.

The implementation also provided practical understanding of CMOS transistor-level design, logic verification, layout generation, and circuit simulation. Microwind was used to study the physical layout and verify the functionality of the designed circuit at the 90nm technology level. Thus, the project demonstrates how a 4:1 multiplexer can be efficiently designed and analyzed using VLSI design tools and serves as a basic building block for more complex digital integrated circuits.

REFERENCES

[1] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson Education.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, Digital Integrated Circuits: A Design Perspective. Pearson Education.
[3] S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design. McGraw-Hill Education.
[4] DSch Digital Schematic Editor, Microwind and DSch VLSI Design Software, used for schematic design and functional simulation of the 4:1 multiplexer.
[5] Microwind VLSI Design Tool, used for CMOS layout design, simulation, and verification of the 4:1 multiplexer using 90 nm technology.
[6] M. M. Mano and M. D. Ciletti, Digital Design. Pearson Education.
[7] A. S. Sedra and K. C. Smith, Microelectronic Circuits. Oxford University Press.
[8] J. Uyemura, CMOS Logic Circuit Design. Springer.
[9] A. P. Chandrakasan and R. W. Brodersen, Low Power Digital CMOS Design. Kluwer Academic Publishers.