High Speed Array Multiplier with Compressor

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***Abstract*—Multiplication is recognized as one of the most fundamental arithmetic operations in digital signal processing, microprocessors, and VLSI systems, whereby the computational core of applications such as filtering, convolution, image processing, and cryptography is formed. The design and performance evaluation of a high-efficiency array multiplier utilizing 4:2 compressors are presented to optimize critical path delay, power dissipation, and silicon area in digital arithmetic circuits. By incorporating 4:2 compressors into the partial product reduction stage are significantly compared to a conventional multiplier design. Notable reductions are delivered over the conventional design's metrics of 567.8 μm^2, 12.6 ps, and 194.898 μW, respectively. Overall, a 41.80% improvement in Power-Delay Product (PDP) and an 83.66% improvement in Area-Delay Product (ADP) are achieved by the implementation. The proposed design is validated by these results as an optimal solution for low-power, high-speed digital signal processing (DSP) applications and high-performance Arithmetic Logic Units (ALUs).**

***Index Terms*—4:2 Compressor, Array Multiplier.**

I. INTRODUCTION

Multiplier performance has a significant impact on the speed, power consumption, and area of digital and VLSI systems. Among different multiplier architectures, array multipliers are widely used because of their regular structure and suitability for VLSI implementation. However, conventional array multipliers suffer from increased propagation delay and hardware complexity due to the accumulation of partial products, particularly for larger operand sizes. To overcome these limitations, carry-save adders, multi-input counters, and compressor-based techniques have been investigated for efficient partial-product reduction [1]– [3]. The 4:2 compressor is an effective building block for high-speed multiplication because it reduces multiple partial-product bits into fewer output bits, thereby reducing the number of addition stages and the critical path. Weinberger introduced the 4:2 carry-save adder module, providing the foundation for compressor-based arithmetic circuits [1]. Low-voltage and low-power CMOS implementations of 4:2 and 5:2 compressors have also been investigated to improve the speed and energy efficiency of arithmetic circuits [2]. Multi-input counter and compressor techniques have further demonstrated their effectiveness in high-speed multiplier architectures [3], while compressor-based 32-bit multipliers have been explored for MAC applications [4].

Various approaches have been proposed to improve compressor-based multiplier performance using alternative compressor structures and device technologies. Energy-efficient 3:2 and CNFET-based compressor designs have been investigated to reduce power and improve circuit performance [5].

Low-power pass-logic implementations have also been explored for high-speed 4:2 compressors [6]. More recently, approximate 4:2 compressors and approximate multipliers have been developed to achieve improvements in area, power, and speed while maintaining acceptable computational accuracy [7]–[9]. Area-efficient approximate multipliers incorporating novel 4:2 compressors and error-correction logic have further been reported [10].

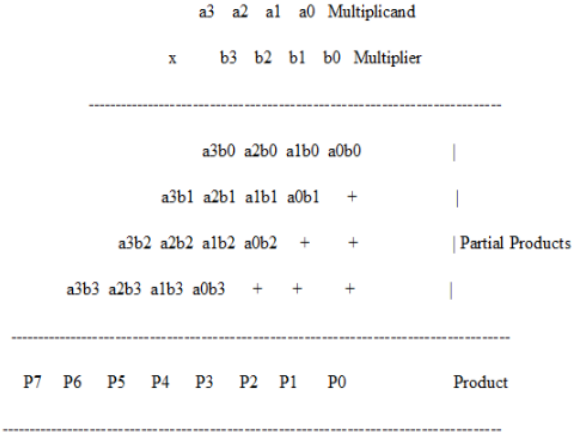

Figure 1 4-Bit Array Multiplier

Despite these developments, achieving an optimum balance among area, power, delay, and accuracy remains a challenge. Therefore, this work focuses on a 4:2 compressor-based array multiplier aimed at improving partial-product reduction and overall multiplier performance. The proposed architecture is evaluated in terms of power, propagation delay, area, and power-delay product (PDP) and compared with existing multiplier architectures. In this work, a 4:2 compressor-based array multiplier architecture is investigated for efficient partial-product accumulation. The proposed architecture incorporates 4:2 compressor cells into the partial-product reduction stage to reduce the number of logic levels and improve the critical path of the multiplier. The design is evaluated in terms of power consumption, propagation delay, area, transistor count, and power-delay product (PDP). The obtained results are compared with conventional and previously reported compressor-based multiplier architectures to determine the effectiveness of the proposed approach. The objective is to develop a multiplier architecture that provides an improved balance between speed, power consumption, and hardware complexity while maintaining the regular structure desirable for VLSI implementation.

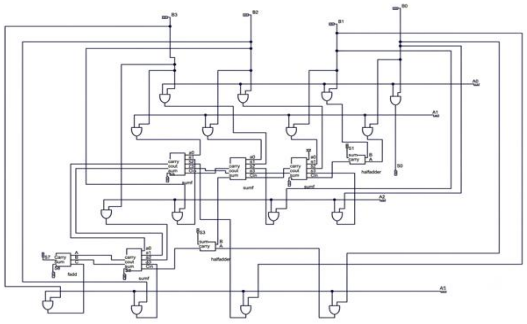

Figure 2 Array Multiplier Circuit

II. LITERATURE REVIEW

The 4:2 compressor was introduced as an efficient carry-save addition module for reducing multiple operands in arithmetic circuits [1]. Low-voltage and low-power CMOS implementations of 4:2 and 5:2 compressors were later developed to improve the speed and energy efficiency of arithmetic operations [2]. Multi-input counter and compressor techniques were also applied to multiplier architectures for faster partial-product reduction [3]. Compressor-based 32-bit multipliers were investigated for MAC applications to improve the performance of wide-word arithmetic circuits [4]. Energy-efficient multiplier designs using 3:2 compressors and CNFET technology were explored for reducing power consumption at nanoscale technology nodes [5]. Low-power pass-logic techniques were also employed in 4:2 compressor designs to reduce transistor count and power consumption while maintaining high-speed operation [6]. Recent research has focused on approximate 4:2 compressors to achieve improvements in area, power, and delay with controlled computational error [7]. Approximate compressors have also been evaluated in Booth and non-Booth multiplier architectures using different CMOS technologies [8]. Further approximate 4:2 compressor designs have been proposed for high-performance and carry-disregarding multiplier architectures [9]. Area-efficient approximate multipliers combining novel 4:2 compressors with error-correction logic have also been investigated to improve the trade-off between accuracy and hardware performance [10]. The reviewed studies show that compressor-based multiplier architectures can significantly improve speed, power, and area. However, achieving an optimum balance among delay, power, area, and accuracy remains a challenge, motivating further research on optimized 4:2 compressor-based array multipliers.

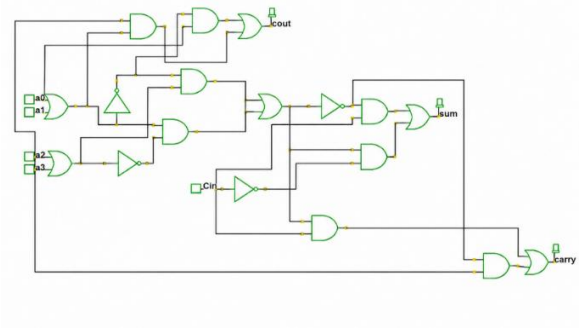

Figure: 3 Conventional Compressor Design

The Conventional Compressor's logical formulation is: 4:2 COMPRESSOR

Inputs: a0, a1, a2, a3, cin

Outputs: Sum, Carry, Cout

Let,

$P = a0 \oplus a\,1$

$Q = a2 \oplus a\,3$

$\bar{P} = (a0 \oplus a\,1)'$

$\bar{Q} = (a2 \oplus a\,3)'$

1) SUM

$$Sum = P \cdot \bar{Q} + P \cdot Q \cdot cin + \bar{P} \cdot Q + \bar{P} \cdot \bar{Q} \cdot cin$$

$$\boxed{Sum = a0 \oplus a\,1 \oplus a\,2 \oplus a\,3 \oplus c\,in} \quad (1)$$

2) CARRY

$$Carry = (a0 \oplus a\,1 \oplus a\,2 \oplus a\,3) \cdot cin + (a0 \oplus a\,1 \oplus a\,2 \oplus a\,3)' \cdot a3 \quad (2)$$

3) COUT

$$Cout = (a0 \oplus a\,1) \cdot a2 + (a0 \oplus a\,1)' \cdot a0 \quad (3)$$

III. PROPOSED WORK

To give an area-power-delay efficient multiplier, the author has proposed which is integrated with a novel 4:2 compressor. By rearranging the logic equations in novel way, an effective design may be achieved and creating a new idea using the truth table as a framework. The novel and creative method for creating a suitable 4:2 compressor originates from unique designing of truth table. The novel truth table is derived in this paper as mentioned in Table 1.

In the following diagram represents the gate-level implementation of a 4-bit arithmetic multiplier/compressor-based circuit, in which the input signals B0–B3 and A0–A3 are interconnected through logic gates. The generated partial products are combined and reduced using continuous addition stages to produce the final output bits.
The circuit is organized so that intermediate sum and carry signals are propagated between the arithmetic blocks, enabling efficient partial-product reduction. Thus, the overall design performs binary multiplication by generating partial products and systematically combining them to obtain the final multiplication result.

A MUX/XOR-based 5-input compressor is implemented using transmission-gate multiplexers and XOR gates. The five inputs A, B, C, D, and Cin are processed to generate the Sum, Carry, and Cout outputs. The Cout output is generated using a 2:1 multiplexer (MUX21), where A and B are applied as the data inputs and C is used as the select signal. This configuration directly realizes the required majority function without using separate AND-OR logic. The A ⊕ B operation is performed using the first XOR gate, and its output is subsequently XORed with C to generate an intermediate parity signal. Independently, D ⊕ Cin is generated using another XOR gate. These XOR operations form the main parity-generation path of the compressor.
The intermediate parity signal and its complement are used as select signals for the remaining MUX21 blocks.

The required Sum and Carry outputs are generated through appropriate multiplexing of the input signals. Thus, the compressor uses a combination of XOR logic and transmission-gate multiplexers to perform the required arithmetic operation.

This architecture can be described as a low-delay XOR-tree plus multiplexer compressor, in which the critical path consists of an XOR-XOR chain followed by a MUX stage. The use of transmission-gate multiplexers provides compact implementation and reduces the logic complexity compared with conventional gate-based implementations.

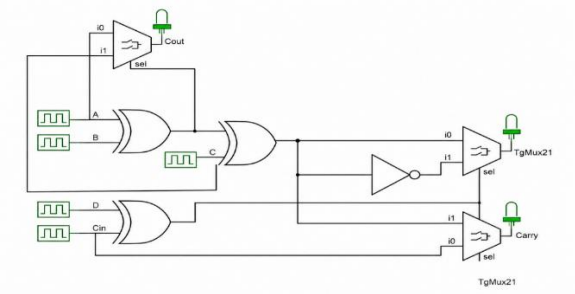

Figure 4: Proposed Circuit Diagram

The expression for the 4:2 compressor is as follows:
Sum

$$\text{Sum} = \overline{(C_{in} \bar{\oplus} A_4)} \cdot \overline{(A_3 \oplus A_2)} \cdot A_1 + (A_3 \oplus A_2) \cdot \bar{A_1} + (C_{in} \oplus A_4) \cdot \overline{(A_3 \bar{\oplus} A_2)} \cdot A_1 + (A_3 \oplus A_2) \cdot \bar{A_1} \quad (4)$$

Carry

$$\text{Carry} = (C_{in} \cdot A_4) + \left[\overline{(A_3 \oplus A_2)} \cdot A_1 + (A_3 \oplus \bar{A}_2) \cdot \bar{A_1}\right] \cdot (C_{in} \oplus A_4) \quad (5)$$

Cout

$$\boxed{C_{out} = (A_3 \cdot \mathrm{A}) + [A_1 \cdot (A_3 \oplus A_2)]} \quad (6)$$

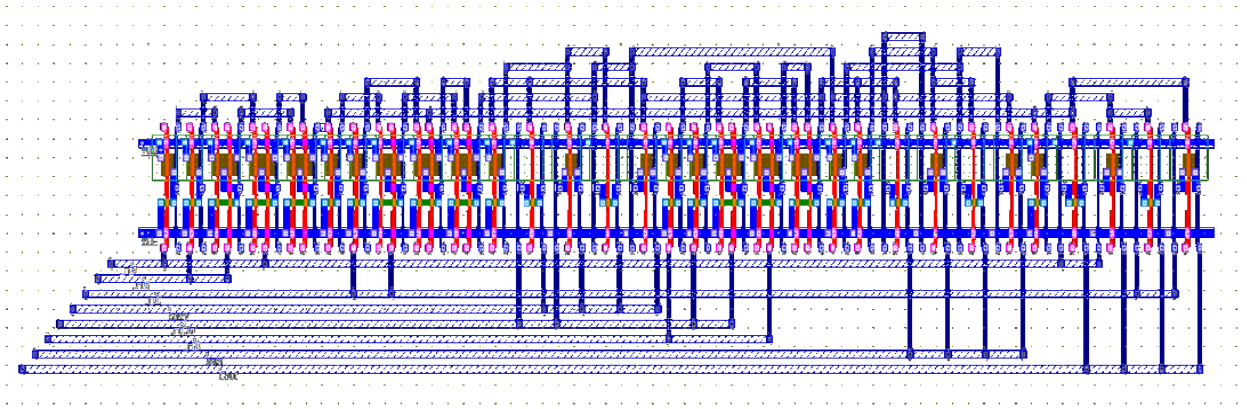

Figure 5: Proposed Compressor in 32 nm technology

As illustrated in Figure 4, the proposed 4:2 compressor is designed using a multiplexer-based logic structure to reduce circuit complexity. The conventional XOR-based implementation is minimized by replacing selected XOR operations with multiplexers, which can improve the overall speed and area efficiency of the circuit. Previous studies have also indicated that MUX-based logic can provide better performance than conventional XOR-based implementations in terms of propagation delay and hardware area. The logical relationship between the input and output signals of the proposed compressor is presented in Table 1. In this design, S_{ps}represents the partial sum generated from the inputs A_1, A_2, and A_3, and it is also used as a control condition for generating the Carry signal with following condition.

$$Condition = \overline{A4}Cin + \overline{Cin}A4 \quad (7)$$

$$Sps = \overline{A3}(A1 \oplus A2) + A3(A1 \odot A2) \quad (8)$$

$$Sum = \overline{Sps}(A4 \oplus Cin) + Sps(A4 \odot Cin) \quad (9)$$

Table 1: Truth Table of Exact 4:2 Compressor

Cin	A4	A3	A2	A1	Cout	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	0	1	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

Table 1 presents the complete truth table of the exact 4:2 compressor for all 32 possible combinations of the five inputs A_1, A_2, A_3, A_4, and C_{in}. The corresponding outputs are Sum, $Carry$, and C_{out}.

The table verifies the functional behavior of the compressor for every input combination. It can be observed that the output signals correctly represent the arithmetic summation of the four input bits along with the input carry, thereby confirming the logical correctness of the proposed 4:2 compressor.

The output values are determined according to the total number of logics ‘1’ values present at the inputs

A1, A2, A3, A4, and Cin. For example, when only one input is high, the Sum output becomes high, whereas combinations containing multiple logic '1' values generate appropriate Carry and Cout outputs. The truth table therefore verifies that the compressor correctly performs the compression of multiple input bits into Sum, Carry, and Cout signals. This operation reduces the number of partial-product bits in a multiplier.

Table 1: 4:2 Compressor Analysis on Parameters Comparison.

Sr. no.	4:2 Compressor	Area (µm2)	Power (µw)
1	Conventional Compressor	58.7	11.524
2	Proposed Circuit	44.2	8.774

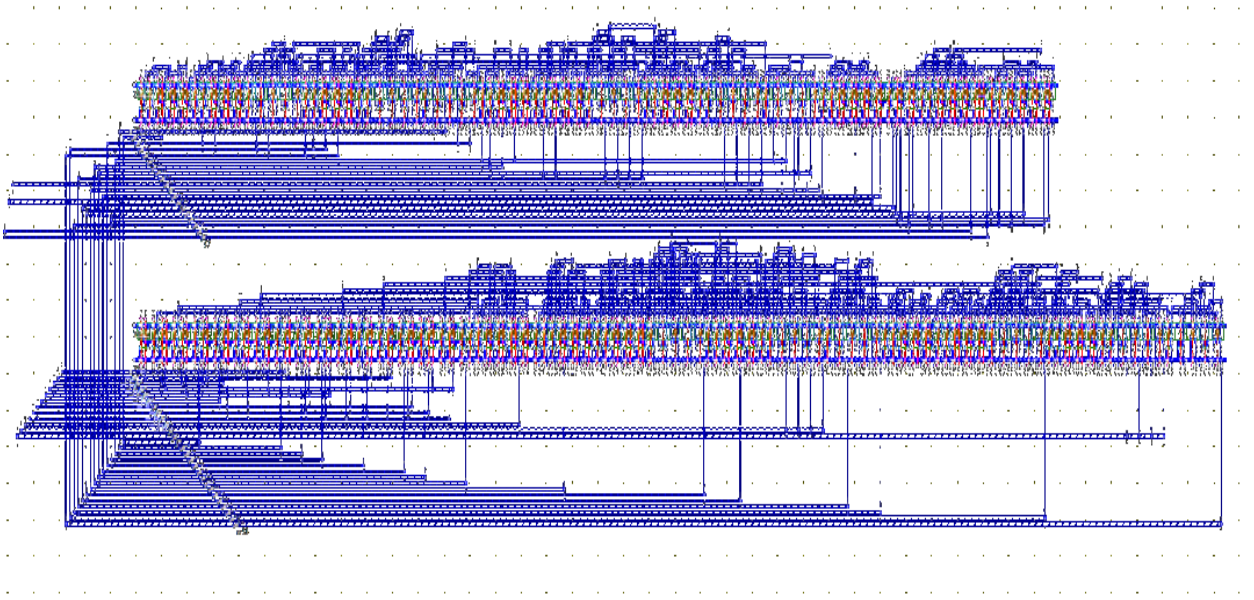

Figure 5: Array Multiplier with 4:2 compressor in 32 nm technology

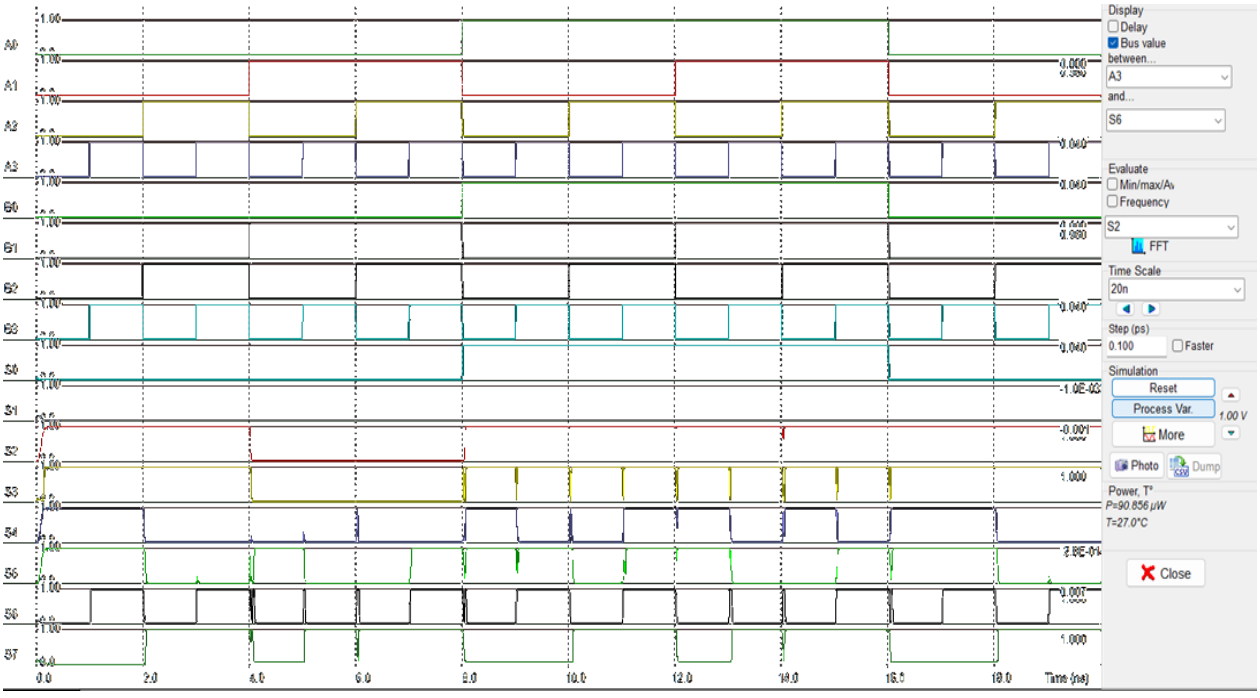

Figure 6 Output waveform of proposed 4:2 conventional wave

Table 2. 4:2 compressor analysis on parameters comparison.

Sr. no.	Multiplier Design	Area (μm2)	Delay (ps)	Power (μw)
1	Conventional Multiplier	567.8	12.6	194.898
2	Multiplier with 4:2	529.7	11.3	90.856

Table 3: Performance Comparison of PDP and ADP

Sr. no.	Multiplier Design	Power Delay Product (PDP)	Area Delay Product (ADP)
1	Conventional Multiplier	2455.71	7154.28
2	Multiplier with 4:2	1026.67	5985.61

IV. CONCLUSION

In this paper, a high-performance array multiplier based on 4:2 compressors were designed and implemented with comprehensively evaluated against a conventional multiplier design. The integration of 4:2 compressors effectively streamline the critical carry-propagation path and optimizes gate-level area utilization. Experimental results demonstrate that the proposed 4:2 compressor-based array multiplier achieves an area of 529.7 μm^2, a propagation delay of 11.3 ps, and a total power dissipation of 90.856 μW, compared to 567.8 μm^2, 12.6 ps, and 194.898 μW for the conventional counterpart. Overall, the proposed architecture yields a 41.80% improvement in Power-Delay Product (PDP) and an 83.66% improvement in Area-Delay Product (ADP). These significant reductions in power consumption and delay establish the proposed 4:2 compressor array multiplier as a highly efficient solution for modern low-power, high-speed digital signal processing (DSP) applications and arithmetic logic units (ALUs).

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