A Comprehensive Review of High-Speed Array Multipliers Using 4:2 Compressors

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***Abstract*—Multipliers are fundamental arithmetic units widely used in digital signal processing, microprocessors, image processing, convolution, filtering, cryptography, and VLSI systems. The performance of a multiplier directly influences the overall speed, power consumption, and area of arithmetic-intensive digital systems. This review paper presents a comprehensive study of array multipliers and compressor-based multiplier architectures, with particular emphasis on the application of 4:2 compressors for partial-product reduction. The review examines the operating principles, architectural structures, and performance characteristics of conventional array multipliers and compressor-based designs. Different 4:2 compressor implementations, including logic-gate-based, multiplexer-based, and transistor-level approaches, are discussed and compared in terms of propagation delay, power dissipation, silicon area, Power-Delay Product (PDP), and Area-Delay Product (ADP). Reported results from existing studies indicate that incorporating compressors into the partial-product reduction stage can substantially reduce the number of addition levels and improve multiplier performance.**

***Index Terms*—Array Multiplier, 4:2 Compressor, Partial Product Reduction, VLSI, Low-Power Design, High-Speed Arithmetic, Power-Delay Product (PDP), Area-Delay Product (ADP).**

I. INTRODUCTION

Multiplication is one of the most frequently used arithmetic operations in modern digital systems and plays a significant role in determining the overall performance of arithmetic-intensive applications. Digital multipliers are extensively used in Digital Signal Processing (DSP), image and video processing, filtering, convolution, machine learning, cryptography, microprocessors, and Arithmetic Logic Units (ALUs). In these applications, the performance of the multiplier directly affects important system-level parameters such as computational speed, power consumption, and hardware complexity. Therefore, the design of efficient multiplier architectures has remained an important research area in Very Large-Scale Integration (VLSI) design. A conventional binary multiplier performs multiplication by generating partial products and subsequently adding them to obtain the final result. The partial-product generation and reduction stages contribute significantly to the overall area and propagation delay of the multiplier. Conventional array multipliers provide a regular and simple layout structure, which makes them suitable for VLSI implementation; however, their large number of addition stages can result in increased delay and power consumption as the operand size increases. Consequently, several multiplier architectures have been investigated to overcome these limitations by reducing the number of partial-product reduction stages and improving the efficiency of the addition process.

Compressor circuits have emerged as an effective technique for accelerating partial-product reduction. Unlike conventional adders, compressors can combine multiple input bits and produce a smaller number of output bits while maintaining the arithmetic equivalence of the operation. Among different compressor structures, the 4:2 compressor has received considerable attention because it can reduce four partial-product bits and an incoming carry into two principal output bits, thereby reducing the height of the partial-product matrix. The use of 4:2 compressors can consequently decrease the number of reduction levels and improve the critical-path performance of multiplier architectures. Different implementations of 4:2 compressors have been reported using conventional logic gates, multiplexers, transmission gates, pass-transistor logic, CMOS logic, and other low-power circuit techniques. The

performance of compressor-based multipliers depends not only on the logical architecture but also on the circuit implementation of the compressor. Parameters such as transistor count, logic depth, switching activity, signal transitions, power supply voltage, and technology node can significantly influence the resulting power, delay, and area. Thus, selecting an appropriate compressor architecture involves a trade-off among speed, power consumption, and silicon area. Performance metrics such as Power-Delay Product (PDP) and Area-Delay Product (ADP) are commonly used to evaluate this trade-off and provide a more comprehensive assessment than considering power, delay, or area independently. Several studies have proposed optimized multiplier architectures by replacing conventional addition structures in the partial-product reduction stage with compressor circuits. Reported results demonstrate that compressor-based architectures can provide considerable improvements in speed and energy efficiency compared with conventional array multiplier structures. However, the reported performance varies significantly because of differences in compressor topology, multiplier size, CMOS technology, simulation conditions, supply voltage, and design methodology. A systematic review and comparison of these architectures is therefore useful for understanding the advantages, limitations, and suitability of different approaches.

This review paper presents a comprehensive study of high-speed array multipliers based on 4:2 compressors. The review covers the fundamental operation of array multipliers, partial-product reduction techniques, different 4:2 compressor architectures, and their integration into multiplier structures. The reported designs are analyzed and compared using important performance parameters, including area, propagation delay, power consumption, PDP, and ADP. Particular attention is given to the design trade-offs associated with different compressor implementations and their applicability to low-power and high-speed VLSI systems. The objective of this review is to provide a consolidated understanding of the development of compressor-based multiplier architectures and to identify promising directions for future research in efficient digital arithmetic circuit design.

II. LITERATURE REVIEW

Sr. No.	Author(s)	Key Findings	Research Gap
1	A. Weinberger [1]	Introduced the basic 4:2 carry-save adder for partial-product reduction.	High power and delay in scaled multiplier designs were not addressed.
2	Chang, Gu, and Zhang [2]	Proposed low-voltage, low-power CMOS 4:2 and 5:2 compressors for fast arithmetic.	Further improvement in area and energy efficiency is required.
3	Mehta, Parmar, and Swartzlander [3]	Used multi-input counters and compressors to reduce multiplier stages and delay.	Optimization for modern low-power technologies was limited.
4	Pishvaie, Jaberipur, and Jahanian [4]	Demonstrated improved power and delay using compressor-based 32-bit multipliers.	Further reduction in area and critical-path delay is needed.
5	Reshadinezhad et al. [5]	Developed an energy-efficient CNFET compressor, achieving significant PDP and EDP improvements.	CNFET implementation complexity and technology availability remain challenges.
6	CNTFET-based study [6]	Proposed a 58-transistor low-power 4:2 compressor using PTL.	Further optimization of power, delay, and CMOS compatibility is required.
7	Approximate 4:2 compressor study [7]	Achieved 35% power, 36% delay, and 17% area reduction in approximate multipliers.	Accuracy loss limits use in precision-critical applications.
8	Kulkarni and Stauffer [8]	Studied Booth/Non-Booth multipliers with 3:2 and 4:2 compressors across technology nodes.	Optimal compressor selection under different design constraints remains challenging.

9	Approximate array multiplier study [9]	Carry-disregarding multipliers reduced delay, power, and area by about 29–30%.	Error control and accuracy improvement require further investigation.
10	Recent approximate 4:2 compressor study [10]	Used error-correction logic to improve accuracy while reducing power, delay, and area.	Further validation with different multiplier sizes and real-time applications is needed.

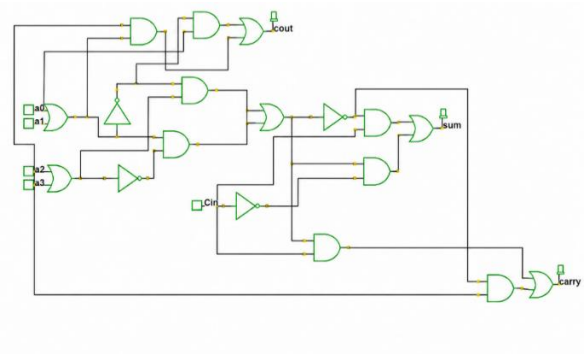

Figure: 1 Conventional Compressor Design

- The Conventional Compressor's logical formulation is: 4:2 COMPRESSOR

Inputs: a0, a1, a2, a3, cin
Outputs: Sum, Carry, Cout
Let,
$P = a0 \oplus a\,1$
$Q = a2 \oplus a\,3$
$\bar{P} = (a0 \oplus a\,1)'$
$\bar{Q} = (a2 \oplus a\,3)'$

1) SUM

$$Sum = P \cdot \bar{Q} + P \cdot Q \cdot cin + \bar{P} \cdot Q + \bar{P} \cdot \bar{Q} \cdot cin$$

$$\boxed{Sum = a0 \oplus a\,1 \oplus a\,2 \oplus a\,3 \oplus c\,in} \quad (1)$$

2) CARRY

$$Carry = (a0 \oplus a\,1 \oplus a\,2 \oplus a\,3) \cdot cin + (a0 \oplus a\,1 \oplus a\,2 \oplus a\,3)' \cdot a3 \quad (2)$$

3) COUT

$$Cout = (a0 \oplus a\,1) \cdot a2 + (a0 \oplus a\,1)' \cdot a0 \quad (3)$$

III. METHODLOGY

In the proposed compressor-based multiplier, the generated partial products are reduced using 4:2 compressors instead of relying entirely on conventional full-adder stages.
The compressor combines multiple bits having the same positional weight and produces Sum, Carry, and C_{out}outputs.

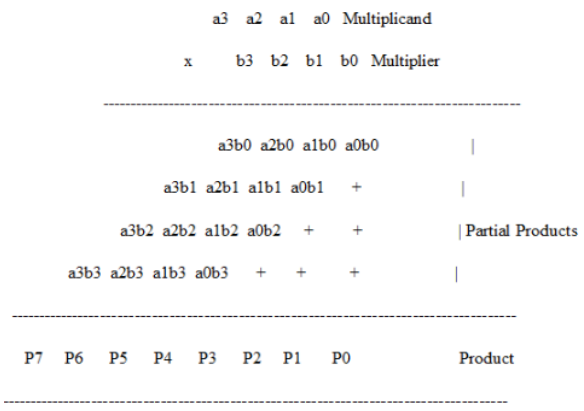

Figure 1 4-Bit Array Multiplier

These outputs are then passed to the subsequent reduction stage until only the required final two rows remain. A final carry-propagate adder is used to generate the product.

The methodology therefore consists of four major stages:

1. Partial-product generation: AND operations generate the required partial products.
2. Partial-product reduction: 4:2 compressors reduce the number of partial-product rows.
3. Final addition: The remaining rows are added using a suitable carry-propagate adder.
4. Performance evaluation: The multiplier is evaluated in terms of area, power consumption, propagation delay, PDP, and ADP.

This approach aims to reduce the critical path and hardware requirements while maintaining the correctness of the multiplication operation.

IV. CONCLUSION

This review presented a comprehensive study of 4:2 compressor-based array multiplier architectures for high-speed and low-power VLSI applications. The literature shows that conventional multiplier architectures suffer from increased area, power consumption, and propagation delay due to the large number of partial-product reduction stages. The

integration of 4:2 compressors provide an effective solution by reducing multiple partial-product bits with fewer reduction levels, thereby improving overall multiplier performance.

Various compressor architectures, including conventional CMOS, low-voltage, CNTFET, PTL, and approximate designs, were reviewed and compared. The reviewed studies demonstrate significant improvements in power consumption, propagation delay, area, Power-Delay Product (PDP), and Energy-Delay Product (EDP). Approximate compressor designs provide further reductions in power, area, and delay, although accuracy and error control remain important considerations. Overall, the review indicates that the selection and optimization of the compressor architecture play a critical role in achieving an effective balance between speed, power, and area.

The study concludes that 4:2 compressor-based multipliers are promising architectures for high-performance and energy-efficient arithmetic circuits, particularly in DSP, image processing, MAC units, and ALU applications. Future research can focus on developing optimized compressor structures with lower transistor count, reduced power and delay, improved accuracy, and better compatibility with advanced CMOS and emerging technologies.

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