

# Active-Clamped Flying-Capacitor Quasi Single-Stage Buck-Boost Inverter

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**Abstract**—This paper reviews the operating concept and mathematical design considerations of an Active-Clamped Flying-Capacitor Quasi Single-Stage Buck-Boost Inverter (AC-FC-QSSBBI) intended for renewable-energy conversion. The supplied dissertation describes a DC input stage, energy-coupling inductance, a bridge switching network, a flying capacitor, an auxiliary active-clamp path, and an output LC filter. The paper develops calculation methods for AC voltage, switching period, ideal buck and boost conversion, inductor-current ripple, capacitor-voltage ripple, flying-capacitor midpoint balancing, LC-filter resonance, total harmonic distortion (THD), and efficiency. Using the stated input voltage of 380 V and switching frequency of 30 kHz, selected numerical examples are calculated transparently. Because the supplied schematic does not provide a complete validated switching-state table or all component/load values, ordinary ideal buck/boost equations are presented as reference models and not claimed as an exact transfer function of the complete inverter. Reported waveform metrics are treated as preliminary values requiring confirmation from steady-state scope traces and FFT measurements.

**Index Terms**—single-stage inverter, buck-boost conversion, flying capacitor, active clamp, PWM, mathematical modeling, LC filter, THD, MATLAB/Simulink.

## I. INTRODUCTION

Renewable sources such as photovoltaic modules can produce a DC voltage that varies with irradiance, temperature, and operating point. An inverter must convert this DC energy to AC while controlling output amplitude, frequency, ripple, and device stress. A conventional two-stage arrangement separates DC-DC voltage adaptation from DC-AC inversion, while a quasi single-stage concept seeks to combine voltage adaptation and inversion in one power-processing structure.

The supplied dissertation proposes an active-clamped flying-capacitor arrangement. The flying capacitor is intended to support voltage sharing and balancing, while the active-clamp branch is intended to limit switching transients. The output LC network attenuates switching-frequency components. These are design objectives; claims such as guaranteed zero-voltage switching, a specific efficiency, or grid-code compliance require switching-state analysis and measurement and are not assumed solely from the topology name.

## II. SYSTEM DESCRIPTION AND MODELING ASSUMPTIONS

The supplied dissertation identifies the following functional elements: DC source  $V_{in}$  and input capacitor  $C_{in}$ ; energy-coupling inductor  $L_1$ ; main bridge switches  $S_1$ – $S_4$ ; auxiliary active-clamp switch SAUX; clamping diode(s); flying capacitor C<sub>FLY</sub>; output filter inductors; output capacitor; and load  $R_L$ . The described control uses PWM with a sinusoidal reference and a high-frequency carrier. The dissertation mentions 30 kHz as a switching-carrier frequency, while its results table separately lists 50 Hz as the fundamental frequency.

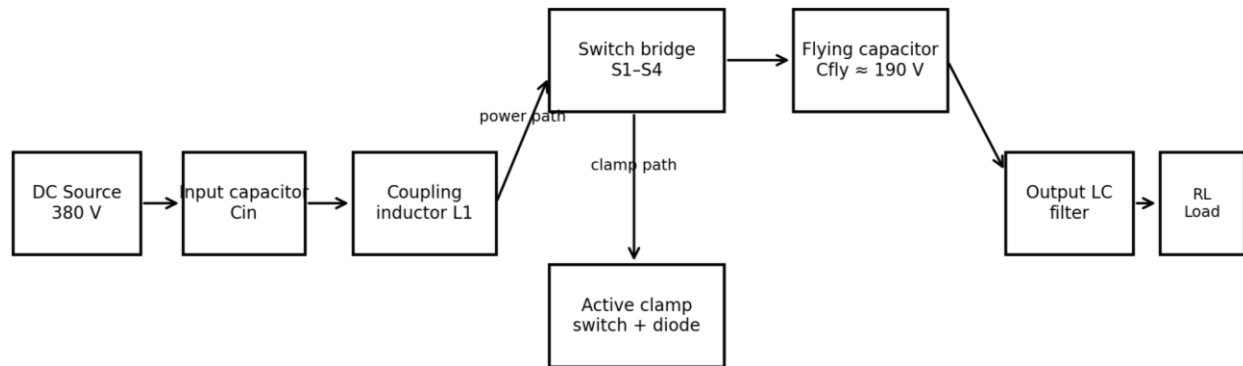
For mathematical clarity, symbols are defined as follows:  $V_{in}$  = DC input voltage;  $V_{dc}$ ,  $o$  = equivalent DC conversion output in an ideal reference converter;  $v_o(t)$  = AC output voltage;  $V_{pk}$  = AC peak voltage;  $V_{rms}$  = RMS voltage;  $D$  = duty ratio;  $f_s$  = switching frequency;  $T_s$  = switching period;  $L$  = inductance;  $C$  = capacitance;  $\Delta i_L$  = peak-to-peak inductor ripple;  $\Delta v_C$  = peak-to-peak capacitor ripple;  $M$  = sinusoidal modulation index.

Important limitation: the ideal buck and boost formulas below are reference equations for conventional non-isolated DC-DC stages. The exact

AC-FC-QSSBBI gain law depends on the actual circuit connections, conducting switches/diodes in each state, and control timing. A topology-specific

averaged model should be derived from those states before using these equations as a final design law.

### Conceptual topology map for MATLAB/Simulink implementation



Note: confirm exact switch/diode polarities and node connections against the original circuit before simulation.

Figure 1. Conceptual MATLAB/Simulink topology diagram

Note: This is a conceptual block diagram, not a validated switch-level schematic. Verify switch/diode directions and node connections against the actual circuit.

### III. MATHEMATICAL ANALYSIS

#### 3.1 AC voltage, RMS value, and fundamental period

For a sinusoidal output voltage:

$$v_o(t) = V_{pk} \sin(2\pi f_o t + \phi)$$

$$V_{rms} = V_{pk} / \sqrt{2} \quad \text{and} \quad V_{pk} = \sqrt{2} V_{rms}$$

$$T_o = 1 / f_o$$

For the target 230 V RMS output:

$$V_{pk} = \sqrt{2} \times 230 = 325.27 \text{ V}$$

$$T_o = 1 / 50 = 0.020 \text{ s} = 20 \text{ ms}$$

Thus, a measured 230 V RMS sinusoid at 50 Hz should have a peak near 325 V. This comparison is valid only when the measured waveform is sufficiently sinusoidal and RMS is measured over an integer number of fundamental cycles.

#### 3.2 Switching frequency and duty ratio

$$T_s = 1 / f_s$$

At the dissertation's stated carrier frequency of 30 kHz:

$$T_s = 1 / 30,000 = 33.33 \mu\text{s}$$

For PWM, the ideal duty ratio is  $D = T_{on}/T_s$ . A 50% pulse width corresponds to  $D = 0.5$  for that pulse. It does not by itself prove that the inverter output is a 50 Hz sinusoid; sinusoidal output normally requires a modulation/reference strategy and correctly coordinated gate signals.

#### 3.3 Reference buck-mode calculation

For an ideal conventional buck converter operating in continuous conduction mode:

$$V_o \approx D V_{in}$$

$$D \approx V_o / V_{in}$$

As an illustrative DC conversion example only, if  $V_{in} = 380 \text{ V}$  and the required equivalent DC output is 325.27 V:

$$D \approx 325.27 / 380 = 0.856 = 85.6\%$$

This is not a direct gate-duty recommendation for the complete inverter: the actual AC peak depends on the inverter modulation index, topology, filter, and switching-state sequence. Do not set the complete inverter to 85.6% from this equation without validating its gain model.

#### 3.4 Reference boost-mode calculation

For an ideal conventional boost converter in continuous conduction mode:

$$V_o \approx V_{in} / (1 - D)$$

$$D \approx 1 - V_{in} / V_o$$

For an illustrative example with  $V_{in} = 250$  V and an equivalent target of 325.27 V:

$$D \approx 1 - (250 / 325.27) = 0.231 = 23.1\%$$

Again, this is a reference DC-DC calculation, not a verified duty ratio for the complete AC-FC-QSSBBI. The inverter's boost operation must be obtained from the actual switch/diode conduction states and averaged inductor volt-second balance.

### 3.5 Inductor-current ripple and inductance sizing

For a conventional buck stage, the approximate inductor current ripple in continuous conduction mode is:

$$\Delta i_L \approx (V_{in} - V_o) D / (L f_s)$$

$$L \approx (V_{in} - V_o) D / (\Delta i_L f_s)$$

For a conventional boost stage:

$$\Delta i_L \approx V_{in} D / (L f_s)$$

$$L \approx V_{in} D / (\Delta i_L f_s)$$

These equations assume ideal components and the corresponding standard converter circuit. They should not be mixed across modes. The supplied dissertation reports  $\Delta i_L \approx 0.55365349$  A, but a reproducible calculation requires the actual inductance, operating mode, input/output voltages, duty ratio, and whether ripple is peak-to-peak. Those complete values are not all specified in the supplied results table.

### 3.6 Capacitor sizing and voltage ripple

A first-order capacitor sizing estimate can be obtained from charge balance:

$$\Delta Q = C \Delta V \Rightarrow C = \Delta Q / \Delta V$$

For a capacitor carrying approximately constant current ripple over a time interval  $\Delta t$ :

$$C \approx I_C \Delta t / \Delta V_C$$

In many converter design estimates, a mode-specific approximation is used. For example, a boost output capacitor under ideal CCM assumptions may be estimated by:

$$C_o \approx I_o D / (f_s \Delta V_o)$$

The exact expression depends on which capacitor is being sized and the topology's charging/discharging intervals. The supplied dissertation reports a minimum ideal capacitance of 14.2963507  $\mu$ F and a ripple voltage of 2.2199627222 V. These are retained as reported values, not independently verified, because the associated current, duty ratio, voltage-ripple

definition, and exact capacitor branch are not completely provided.

### 3.7 Flying-capacitor midpoint balancing

For a three-level arrangement intended to divide a DC bus equally, the ideal midpoint target is:

$$V_{CFLY, ref} = V_{in} / 2$$

$$\text{For } V_{in} = 380 \text{ V: } V_{CFLY, ref} = 380 / 2 = 190 \text{ V}$$

A simple balancing error signal can be defined as:

$$e_C(t) = V_{CFLY, ref} - V_{CFLY}(t)$$

A controller may use  $e_C$  to adjust redundant switching-state dwell times or a modulation offset. The sign and magnitude of that adjustment must be mapped to the actual circuit's charging states; a generic proportional correction is not enough to prove stable balancing. The dissertation's statement that the capacitor is maintained at 190 V should be confirmed by plotting the measured capacitor voltage with readable axes and reporting its average and peak-to-peak ripple.

### 3.8 LC output-filter resonance

For an ideal second-order LC low-pass filter, the undamped natural resonant frequency is:

$$f_r = 1 / (2\pi \sqrt{LC})$$

The selected L and C should attenuate the switching component around 30 kHz while allowing the 50 Hz fundamental to pass with acceptable amplitude and phase change. The numerical resonance cannot be calculated from the supplied material because the final filter inductance and capacitance values are not fully specified together. Practical design must also check damping, load dependence, inductor current rating, capacitor ripple current, and control-loop stability.

### 3.9 THD and RMS error

For a periodic voltage containing a fundamental component and harmonics, voltage THD is defined as:

$$THD_V (\%) = 100 \times \sqrt{(V_2^2 + V_3^2 + \dots + V_n^2)} / V_1$$

Here  $V_1$  is the RMS magnitude of the fundamental and  $V_2 \dots V_n$  are RMS harmonic magnitudes.

The FFT window, number of cycles, sampling rate, and harmonic range must be stated. A scope screenshot alone is not enough to verify a THD number.

$$RMS \text{ error } (\%) = 100 \times |V_{rms, meas} - V_{rms, target}| / V_{rms, target}$$

If a measured RMS output is 230 V and the target is 230 V, the RMS error is 0%. If the reported filtered

output is 230 V RMS, that arithmetic matches the target; its validity still depends on the measurement block and steady-state data.

### 3.10 Efficiency calculation

$$\eta (\%) = 100 \times P_{\text{out}} / P_{\text{in}}$$

Input and output real power should be measured over the same steady-state interval. For AC output,  $P_{\text{out}}$  should use the average instantaneous power  $v(t)i(t)$ , not simply  $V_{\text{rms}} \times I_{\text{rms}}$  unless power factor is unity. The supplied dissertation includes estimated efficiency claims above 95% and a projected 97.8%; these are not treated as measured results in this paper without input/output power data.

## IV. SIMULATION SETUP AND REPORTED PARAMETERS

| Parameter                    | Value in supplied dissertation | Comment                                             |
|------------------------------|--------------------------------|-----------------------------------------------------|
| DC input voltage             | 380 V                          | Reported simulation setting                         |
| Fundamental output frequency | 50 Hz                          | Target fundamental                                  |
| Switching carrier frequency  | 30 kHz                         | Used in the mathematical examples                   |
| Pulse width                  | 50%                            | Reported setting; gate coordination must be checked |
| Phase delay                  | 0.01 s                         | Needs clarification against 50 Hz period (20 ms)    |
| Flying-capacitor target      | 190 V                          | Half of 380 V input                                 |
| Reported inductor ripple     | 0.55365349 A                   | Underlying parameter set needs verification         |
| Reported minimum capacitance | 14.2963507 $\mu\text{F}$       | Underlying derivation needs verification            |
| Reported capacitor ripple    | 2.2199627222 V                 | Measurement definition should be documented         |

## V. BUCK AND BOOST OPERATING CONCEPTS

### 5.1 Buck region

In a buck region, the source is above the desired equivalent conversion level. During the active interval, the energy-transfer inductor is energized from the source; during the freewheeling interval, its current continues through the permitted diode/switch path. In steady state, the inductor's average voltage over a switching period is zero:

$$\langle v_L \rangle_{T_s} = 0$$

For the conventional buck reference circuit, this produces  $V_o \approx D V_{\text{in}}$ . For the proposed inverter, the exact conducting devices and output polarity must be read from the actual schematic before writing topology-specific state equations.

### 5.2 Boost region

In a boost region, the source is below the desired equivalent conversion level. The inductor stores energy during one switching state and transfers energy to the output during another. Applying inductor volt-second balance to an ideal conventional boost stage gives:

$$D V_{\text{in}} + (1 - D) (V_{\text{in}} - V_o) = 0$$

$$\Rightarrow V_o = V_{\text{in}} / (1 - D)$$

This relation is a conventional boost reference. The actual AC-FC-QSSBBI may have additional capacitor and switch states, so its gain should be derived from a complete state table rather than assumed to follow the basic boost equation.

## VI. PRELIMINARY RESULTS AND DISCUSSION

| Metric                | Unfiltered value (reported) | Filtered value (reported) | Interpretation / verification                                   |
|-----------------------|-----------------------------|---------------------------|-----------------------------------------------------------------|
| Peak voltage          | 380 V                       | 325 V                     | 325 V is consistent with approximately 230 V RMS for a sinusoid |
| RMS voltage           | 268 V                       | 230 V                     | Verify using a steady-state RMS measurement block               |
| Fundamental frequency | 50 Hz                       | 50 Hz                     | Verify by measuring                                             |

|     |      |       |                                                           |
|-----|------|-------|-----------------------------------------------------------|
|     |      |       | cycle period over several cycles                          |
| THD | ≈45% | <3.5% | Requires FFT report; not verifiable from screenshot alone |

The supplied dissertation labels Scope-01 as flying-capacitor voltage balancing, Scope-02 as unfiltered output voltage, Scope-03 as active-clamp switching pulses, and Scope-04 as filtered output voltage. The intended interpretation is that the flying capacitor

approaches half the input voltage, gate pulses control switching states, and the output filter attenuates high-frequency ripple. The screenshots provided in the project context are not sufficiently legible at the displayed scale to independently confirm all numerical claims.

The target of less than 5% THD is presented here only as the project's stated comparison target. IEEE 519 applicability depends on the point of common coupling, system voltage, current distortion metric, and the applicable edition/limits; a voltage THD value alone does not establish compliance.

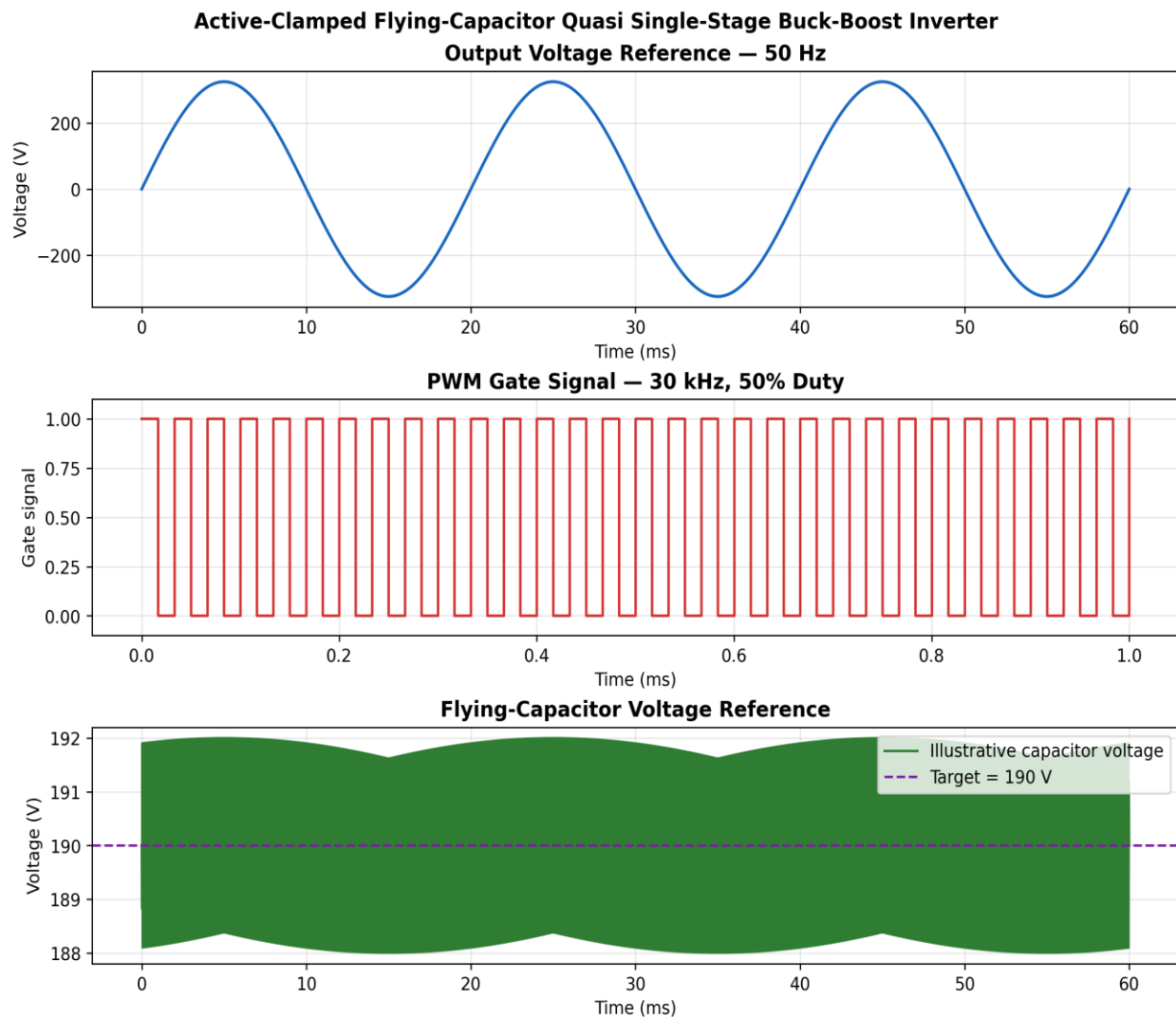


Figure 2. Coloured illustrative waveform references

Note: These coloured plots are illustrative reference waveforms, not direct MATLAB/Simulink exports.

Replace them with actual Scope and FFT/THD results before formal submission.

## VII. DESIGN AND VALIDATION PROCEDURE

- Document the exact circuit topology, device orientation, component values, and measurement points.
- Create a switching-state table for each active and freewheeling interval, including the active clamp and flying-capacitor current direction.
- Derive the state equations and average them over a switching period; check inductor volt-second balance and capacitor charge balance.
- Set the simulation solver, switching frequency, fundamental reference, load, and simulation stop time explicitly.
- Run the model until steady state, then record input voltage/current, output voltage/current, flying-capacitor voltage, and switch stresses.
- Use an RMS measurement over an integer number of 50 Hz cycles and an FFT window that excludes startup transients.
- Calculate real input/output power and efficiency; report component losses if available.
- Repeat across input-voltage and load variations to test both buck and boost regions.

## VIII. LIMITATIONS

This work is a simulation-oriented mathematical review based on the supplied dissertation. The complete topology-specific switching sequence, all component values, load value, controller membership functions/rule table, readable steady-state waveforms, and FFT output were not fully available in the supplied text. Consequently, the conventional buck/boost formulas are explicitly identified as reference models, and reported ripple/THD/efficiency values are not represented as independently validated. Experimental hardware results are outside the evidence provided.

## IX. CONCLUSION

This paper organizes the AC-FC-QSSBBI concept and supplies a mathematical framework for voltage conversion, PWM timing, inductor and capacitor sizing, flying-capacitor balancing, LC-filter design, THD, and efficiency. For the stated 380 V DC input, the ideal half-bus flying-capacitor target is 190 V; a 230 V RMS sinusoidal output corresponds to a peak of

about 325.27 V and a 50 Hz period of 20 ms. A 30 kHz switching frequency corresponds to a switching period of 33.33  $\mu$ s. These calculations are directly reproducible. However, exact buck/boost duty ratios and claims of high efficiency, zero-voltage switching, or grid compliance must be confirmed using the actual switching-state model and verified simulation measurements.

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