Design and Performance Analysis of a High-Gain Cascode Current-Mirror Operational Amplifier for Three 4-Bit DAC Architectures in 180-nm CMOS Technology

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***Abstract*—Digital-to-analog converters (DACs) are important building blocks in mixed-signal systems, where conversion accuracy depends on the DAC architecture and the analog circuitry used at its output. This paper presents a simulation-based study of a redesigned cascode current-mirror operational amplifier and its use in three 4-bit DAC architectures: binary-weighted, R–2R ladder, and current-steering DACs. The circuits are implemented in a 180-nm CMOS technology environment using Cadence Virtuoso, with a reported supply voltage of 2.5 V for the proposed design. The simulated low-frequency gain of the redesigned operational amplifier is approximately 70.65 dB, based on the AC-response marker. The amplifier is then used in the three DAC implementations, whose transient output waveforms are examined across the 16 input codes. Integral nonlinearity (INL) and differential nonlinearity (DNL) are evaluated using an endpoint-fit reference derived from the measured endpoint voltages. The current screenshot-transcribed dataset indicates lower INL and DNL deviations for the current-steering implementation than for the binary-weighted and R–2R implementations. These numerical linearity results remain provisional pending verification of all settled output-code voltages and code-to-waveform mapping. The op-amp power consumption has not yet been measured and is not used to claim a power-efficiency improvement. Since the reference study used a 1.8-V supply, its reported gain is presented as a contextual benchmark rather than a controlled, supply-matched comparison.**

***Index Terms*—Cascode current mirror, CMOS operational amplifier, 180-nm CMOS, digital-to-analog converter, binary-weighted DAC, R–2R ladder DAC, current-steering DAC, integral nonlinearity, differential nonlinearity.**

I. INTRODUCTION

Digital-to-analog converters translate digital codes into analog signals and are used in mixed-signal interfaces, signal-generation circuits, and data-conversion systems. The choice of DAC architecture affects circuit complexity, output range, matching requirements, switching behavior, and conversion linearity [1], [2]. The analog circuitry surrounding a DAC can also influence the observed output response through finite gain, loading, settling behavior, and nonideal device characteristics [3].

The reference study, "Enhanced Gain and Power Efficiency in CMOS Amplifiers for DAC Applications Using Cascode Current Mirror in 180nm Technology," compared several CMOS amplifier topologies and reported a gain of 61.421 dB for a two-stage operational amplifier employing cascode current mirrors [4]. That work demonstrated the amplifier in a 4-bit binary-weighted DAC. The present work extends the circuit-level investigation by redesigning the cascode current-mirror operational amplifier and applying it to three DAC architectures: binary-weighted, R–2R ladder, and current-steering.

The redesigned amplifier's AC-response plot shows a low-frequency gain marker of approximately 70.6507 dB at 1.51356 Hz. The proposed circuits are reported to use a 2.5-V supply, whereas the reference study used 1.8 V. Consequently, the gain values are not a supply-matched comparison, and the observed difference cannot be attributed exclusively to the topology redesign without further controlled simulations.

The objectives of this work are:

1) To redesign and characterize a cascode current-mirror operational amplifier in a 180-nm CMOS environment.
2) To implement the amplifier in three 4-bit DAC architectures.
3) To evaluate the transient conversion characteristics across all 16 input codes.
4) To compare the architectures using endpoint-fit INL and DNL.

The remainder of the paper describes the circuit methodology, reports the current simulation observations, discusses the limitations of the available measurements, and outlines further characterization required for a complete performance comparison.

II. LITERATURE SURVEY

DAC architectures have been studied extensively because their topology determines component matching requirements, switching behavior, output range, speed, and achievable linearity. Binary-weighted networks offer a direct representation of bit significance, but their implementation requires a wide range of accurately controlled component values. R–2R ladders reduce the number of distinct resistor values to R and 2R, which can simplify layout and matching compared with a fully binary-weighted resistor network. Current-steering DACs select weighted current sources through switches and are widely considered where speed and switching behavior are important. General treatments of data conversion and analog integrated-circuit design describe these trade-offs and the effects of nonideal analog circuitry [1]–[3], [5], [7].

Operational-amplifier gain and output resistance affect closed-loop accuracy and settling when an amplifier is used in a DAC output stage. Cascode devices can increase the effective output resistance and hence the gain, although the achievable benefit depends on supply voltage, device headroom, bias current, and loading [3], [5]. The reference study by Nangare et al. reported a cascode-current-mirror amplifier and a 4-bit binary-weighted DAC in a 180-nm technology environment [4]. The present work extends that circuit-level study by examining binary-weighted, R–2R ladder, and current-steering 4-bit DACs with the redesigned amplifier and comparing their preliminary endpoint-fit INL/DNL results.

The research gap addressed here is not the invention of these established DAC topologies. Rather, it is a common simulation study of three architectures using the authors' redesigned amplifier in one reported 180-nm design environment. Because the reference and proposed amplifier results use different supply voltages, and because some DAC samples were transcribed from screenshots, the present comparison istreated as preliminary rather than a fully controlled benchmark.

III. PROPOSED DESIGN AND METHODOLOGY

A. Overall Design Flow

Figure 1 summarizes the simulation workflow. The amplifier is characterized independently using an AC analysis, after which it is incorporated into the three DAC implementations. Transient output values are collected for the 16 input codes and used to estimate endpoint-fit INL and DNL. The figure is a conceptual workflow diagram; the transistor-level schematics are shown separately in Figs. 2, 4, 6, and 8.

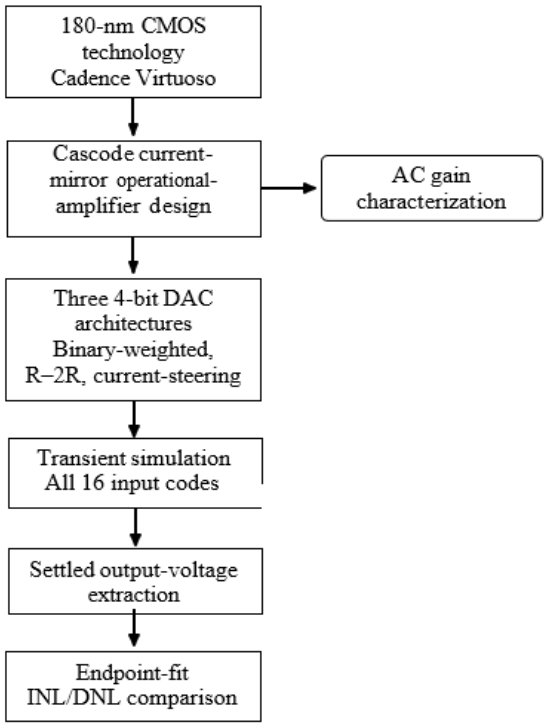


Fig. 1. Overall simulation and analysis flow used in this study. AC gain characterization is performed separately from the transient analysis of the three DAC architectures

B. Technology and Simulation Environment

The circuits were designed and simulated in Cadence Vir¬tuoso using a 180-nm CMOS process. The supply voltage reported for the proposed design is 2.5 V. The reference paper used a 1.8-V supply; this difference is retained explicitly when comparing the two studies. The exact transistor dimensions, bias settings, reference levels, passive component values, out¬put loading, and transient input timing should be reported from the final Cadence testbenches to support reproducibility.

C. Redesigned Cascode Current-Mirror Operational Amplifier

The proposed amplifier uses a differential input stage and current-mirror loading, with cascode devices employed in the gain stages to increase effective output resistance. In a small-signal approximation, the voltage gain of a gain stage is related to its transconductance and effective output resistance:

$$A_v \approx g_m R_{\text{out}}, \quad (1)$$

where gm is the effective transconductance and Rout is the small-signal output resistance [3], [5].

The transistor-level schematic and symbol/testbench are shown in Fig. 2. The AC-response plot in Fig. 3 contains a marker at 1.51356 Hz with a gain of 70.6507 dB. This value is treated as the observed low-frequency gain from the supplied simulation plot. Additional characterization, including power consumption, bandwidth, phase margin, slew rate, and output swing, is needed before making broader claims about the amplifier's overall performance.

For context, the reference paper reports 61.421 dB at 1.8 V [4]. The numerical difference between the reported values is

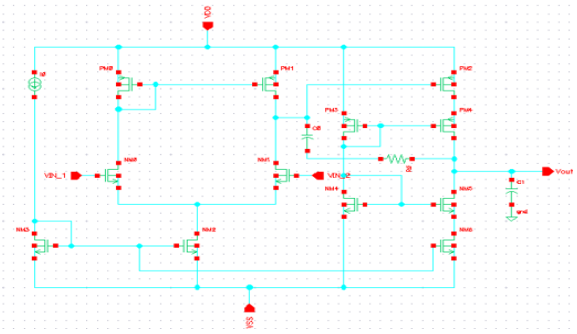


Fig. 2. Transistor-level schematic of the redesigned cascode current-mirror operational amplifier.

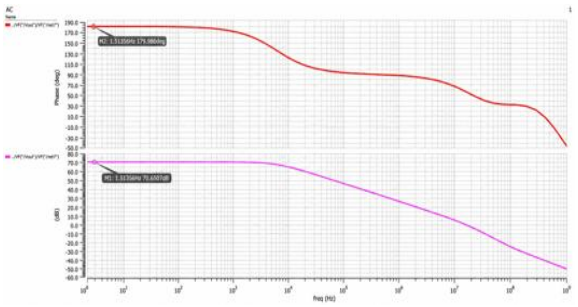


Fig. 3. AC response of the redesigned operational amplifier; the supplied marker indicates approximately 70.65 dB at 1.51356 Hz.

$$\Delta A_v = 70.6507 - 61.421 = 9.2297 \text{ dB}. \quad (2)$$

This is a difference between reported simulation results under different stated supply conditions, not a controlled estimate of improvement caused only by the redesign.

D. 4-Bit Binary-Weighted DAC

The binary-weighted DAC combines contributions from four digital input bits using binary-scaled weights, a conventional DAC approach described in data-conversion references [1], [2]. Ideally, each bit contributes according to its significance, with the most significant bit providing the largest contribution and the least significant bit the smallest. The circuit schematic and supplied transient output are shown in Fig. 4. The output is observed to change in a staircase-like manner as the input code changes.

The exact resistor ratios and mapping between the input waveforms and decimal codes must be confirmed from the final schematic and testbench. This is particularly important because the binary-weighted architecture depends on the intended relative bit weights.

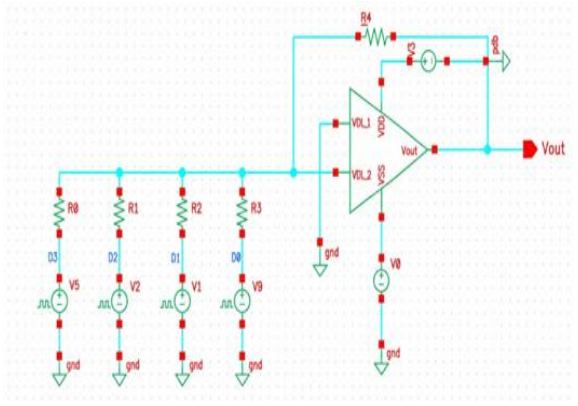


Fig. 4. Schematic of the 4-bit binary-weighted DAC.

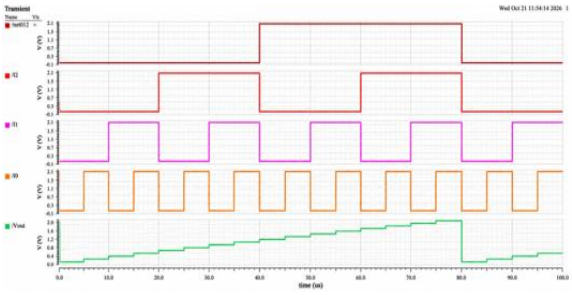


Fig. 5. Supplied transient output waveform for the binary-weighted DAC.

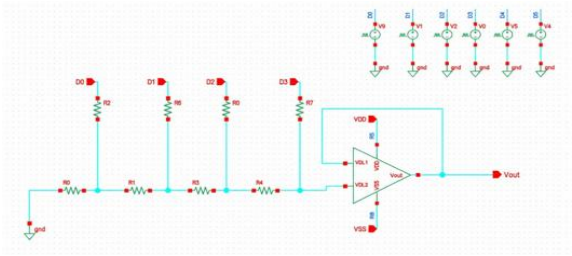


Fig. 6. Schematic of the 4-bit R–2R ladder DAC.

E. 4-Bit R–2R Ladder DAC

The R–2R ladder DAC uses a resistor network with two nominal resistance values, R and 2R, to produce binary-weighted contributions from the digital input bits [1], [2]. The proposed circuit and its transient response are shown in Fig. 6. The observed output follows a staircase-like response across the input sequence. The resistor values, output loading, and op-amp connection should be stated explicitly in the final version.

F. 4-Bit Current-Steering DAC

The current-steering DAC uses controlled switching branches to select and combine current contributions according to the digital input code [1], [2]. The circuit and supplied transient response are shown in Fig. 8. The output changes with the input sequence. The current-source weights, switching arrangement, and the role of the operational amplifier in the

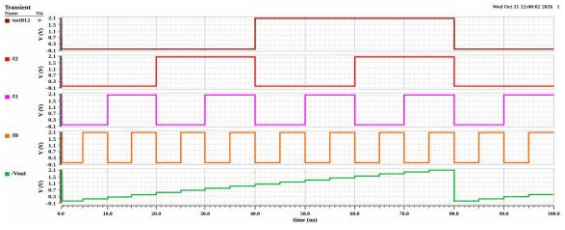


Fig. 7. Supplied transient output waveform for the R–2R ladder DAC.

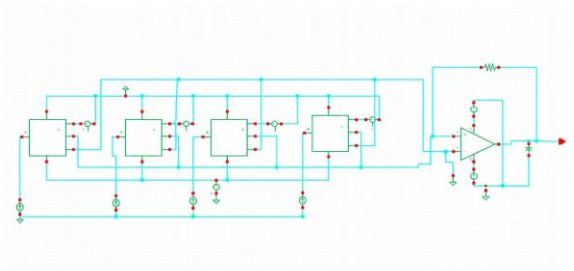


Fig. 8. Schematic of the 4-bit current-steering DAC.

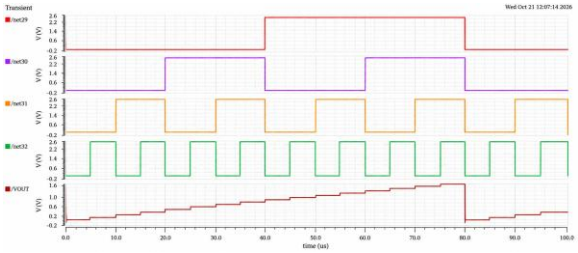


Fig. 9. Supplied transient output waveform for the current-steering DAC.

output stage should be documented according to the final schematic.

G. INL and DNL Calculation

For a 4-bit DAC, there are $2^4 = 16$ digital input codes, from decimal 0 to 15. Let V_k be the settled output voltage measured at code k. The endpoint-fit least significant bit (LSB) is defined as follows [1], [6]:

$$V_{\mathrm{LSB}} = \frac{V_{15} - V_0}{15}. \tag{3}$$

The endpoint-fit ideal output at code k is

$$V_{\mathrm{ideal}}(k) = V_0 + kV_{\mathrm{LSB}}. \tag{4}$$

The endpoint-fit integral nonlinearity is calculated as

$$\mathrm{INL}(k) = \frac{V_k - V_{\mathrm{ideal}}(k)}{V_{\mathrm{LSB}}}. \tag{5}$$

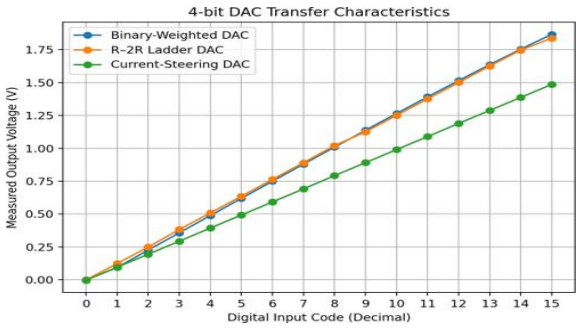


Fig. 10. Comparison of the supplied 4-bit DAC transfer characteristics. The voltage samples should be verified against settled Cadence results before final publication.

The differential nonlinearity for transition k to k + 1 is

$$\mathrm{DNL}(k) = \frac{V_{k+1} - V_k}{V_{\mathrm{LSB}}} - 1, \quad k = 0, \ldots, 14. \qquad (6)$$

INL and DNL are reported in LSB units [1], [6]. The endpoint-fit method removes endpoint offset and gain error from the INL reference, so these metrics should not be interpreted as absolute gain or offset accuracy. For valid comparison, each output sample must correspond to the correct decimal input code and must be measured after the transient response has settled.

IV. RESULTS AND DISCUSSION

A. Operational Amplifier Gain

The supplied AC response indicates a low-frequency gain of approximately 70.6507 dB at 1.51356 Hz. The reference study reported 61.421 dB for its two-stage cascode current-mirror operational amplifier [4]. The difference between the reported gain values is approximately 9.23 dB. Because the proposed circuit is reported at 2.5 V and the reference at 1.8 V, the comparison is contextual and does not isolate the impact of topology changes. A fair comparison would simulate both designs under matching supply, bias, load, and measurement conditions.

B. DAC Transfer Characteristics

The supplied transient plots show staircase-like output be¬havior for all three DACs. The accompanying spreadsheet contains 16 voltage samples per DAC, transcribed from the screenshots. Those samples provide an initial basis for plotting the transfer characteristics and calculating endpoint-fit INL and DNL, but the workbook itself flags the samples as provisional. The marker-to-code mapping and settled output values, especially for the binary-weighted

Table I
Preliminary Endpoint-Fit Linearity Results

Metric	Binary weighted	R–2R ladder	Current steering
Endpoint-fit LSB (V)	0.12442	0.12251	0.09921
Maximum |INL| (LSB)	0.243	0.332	0.0164
Maximum |DNL| (LSB)	0.243	0.256	0.0163
Minimum DNL (LSB)	−0.243	−0.256	−0.0115
Output at code 0 (V)	0.00000	−0.00060	−0.00288
Output at code 15 (V)	1.86632	1.83712	1.48533

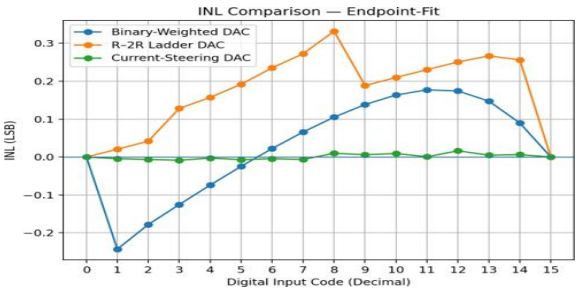


Fig. 11. Supplied endpoint-fit INL comparison for the three DAC architectures.

C. Preliminary INL and DNL Comparison

Using the screenshot-transcribed spreadsheet values and the endpoint-fit definitions above, the preliminary metrics are summarized in Table I. These values are included for analysis planning and must be replaced or confirmed using the final settled output samples.

The preliminary data indicate that the current-steering implementation has the smallest maximum absolute INL and DNL of the three supplied implementations. Its full-scale output is also lower than those of the binary-weighted and R–2R implementations. The difference in output ranges means that linearity alone does not establish which DAC is best overall; output range, power, settling time, and implementation complexity should also be considered.

The supplied INL and DNL plots are reproduced in Figs. 11 and 12. The plotted values should be regenerated from the final verified output-code data before publication.

D. Limitations and Further Characterization

The current results are limited by the use of screenshot-transcribed output voltages and the lack of a measured operational-amplifier power value. The supply voltage differs from that of the reference study. Before drawing final conclusions, the following should be completed:

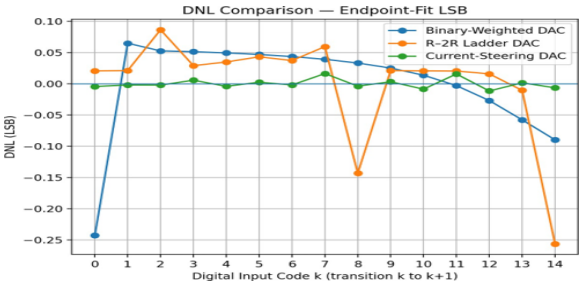


Fig. 12. Supplied endpoint-fit DNL comparison for the three DAC architectures.

1) Verify all 16 settled output voltages for each DAC and confirm code ordering.
2) Confirm the resistor ratios, current weights, reference levels, and output loading for each circuit.
3) Regenerate INL and DNL plots from the verified data using the stated endpoint-fit method.
4) Measure op-amp power consumption and, where feasible, DAC power under clearly defined conditions.
5) Characterize relevant amplifier parameters such as bandwidth, phase margin, and output swing.
6) Compare the reference and redesigned amplifier under matching supply, bias, and loading conditions if attributing a gain improvement to the redesign.

V. CONCLUSION

This paper presents a simulation-based extension of a cascode current-mirror operational amplifier design for DAC applications in 180-nm CMOS technology. The supplied AC-response plot indicates a low-frequency gain of approximately
70.65 dB for the redesigned amplifier at a reported supply voltage of 2.5 V. The amplifier is applied to three 4-bit DAC architectures: binary-weighted, R–2R ladder, and current-steering. Their transient output waveforms exhibit code-dependent staircase behavior. Preliminary endpoint-fit calculations based on screenshot-transcribed voltage samples indicate that the current-steering implementation has the smallest maximum absolute INL and DNL among the three supplied implementations. However, its output range is lower, and the numerical linearity values require verification against settled Cadence output samples and the correct input-code mapping. The reference amplifier's reported gain of 61.421 dB was obtained at 1.8 V, so the difference from the proposed result is not a supply-matched comparison. Power consumption has not yet been measured; therefore, no power-efficiency improvement is claimed.

The study provides a basis for a more complete comparison of the three DAC architectures using verified output data and consistent simulation conditions. Future work will include power measurement, verification of the DAC code-to-output mapping, and additional amplifier and DAC characterization.

VI. FUTURE SCOPE

The present study can be extended in several directions. First, all 16 output-code voltages should be exported directly from Cadence after settling, and the code-to-waveform mapping should be verified before recalculating INL and DNL. Second, amplifier power, unity-gain bandwidth, phase margin, slew rate, output swing, and settling time should be measured under documented bias and load conditions. Third, the proposed and reference amplifier circuits should be simulated with matched supply voltage, process models, bias current, and output loading to make a fair gain comparison. Fourth, mismatch and process-voltage-temperature (PVT) analyses can be performed to study robustness. Finally, the DAC architectures can be compared using a consistent set of metrics, including full-scale range, monotonicity, INL, DNL, settling time, power, and layout area. These investigations would provide a more complete basis for selecting a DAC architecture for a target mixed-signal application.

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