Design and Performance Analysis of a StrongARM Latch-Based 3-bit Flash ADC Compared with an Op-Amp-Based Comparator Flash ADC in 180 nm CMOS

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***Abstract*—Flash analog-to-digital converters (ADCs) require $2^N - 1$ comparators, so comparator power, speed, offset and area dominate converter performance. This paper presents the design and comparative analysis of a 3-bit Flash ADC using a StrongARM latch comparator and the same ADC using a conventional op-amp-based (continuous-time) comparator. Both designs are implemented in Cadence Virtuoso using the GPDK180 (180 nm) process at a supply voltage of 1.8 V and are simulated under identical conditions. The StrongARM-based ADC achieves a total power of 172 µW at 100 MHz, a maximum sampling frequency of 800 MHz, a maximum DNL/INL of 0.31/0.19 LSB and an input-referred offset σ of 9 mV. The op-amp-based design achieves 186 µW, 40 kHz, 0.63/0.37 LSB and 20 mV, respectively. The StrongARM design is about 8 % lower in power at 100 MHz, more than four orders of magnitude faster, and has lower offset and better linearity.**

***Index Terms*—Flash ADC, StrongARM latch, dynamic comparator, op-amp comparator, offset, kickback noise, GPDK180, Monte Carlo analysis.**

I. INTRODUCTION

HIGH-SPEED ADCs are used in communication receivers, data acquisition systems and storage channels. The Flash architecture is the fastest ADC topology because all decisions are made in parallel, but an N-bit Flash ADC needs $2^N - 1$ comparators. Any difference in comparator power or area is therefore multiplied across the whole converter.

Two comparator types are considered in this work. The conventional comparator is an op-amp operated open-loop, which amplifies the input difference continuously to a logic level [1]; it needs no clock but draws static bias current. The StrongARM latch is a dynamic comparator that has no static current and regenerates directly from the input pair [2], [3]. The trade-offs between the two, namely power, speed, offset and kickback noise, strongly affect the overall ADC.

The contributions of this paper are threefold. First, a StrongARM comparator and a conventional op-amp-based comparator are designed in GPDK180. Second, each comparator is integrated into an identical 3-bit Flash ADC consisting of a resistor ladder and a thermometer-to-binary encoder. Third, a like-for-like comparison of power, delay, maximum sampling rate, DNL/INL, offset and kickback noise is presented.

The rest of the paper is organized as follows. Section II reviews related work on Flash ADCs and StrongARM comparator design. Section III describes the architecture and the two comparators. Section IV describes the simulation setup, Section V presents the results, and Section VI concludes the paper.

II. LITERATURE REVIEW

This section reviews prior work that is relevant to the present study. Flash ADC architectures are discussed first, followed by StrongARM latch comparator design and, for comparison, continuous-time op-amp comparators.

A. Flash ADC Architectures

The Flash architecture performs a conversion in a single step by comparing the input with $2^N - 1$

reference levels in parallel, which makes it the usual choice when very high conversion rates are required [4]. Its drawbacks are well known: the number of comparators, the input capacitance and the power all grow exponentially with resolution, and the offset of each comparator limits the linearity that can be reached [4]. CMOS Flash converters with 6-bit resolution and sampling rates above 1 GS/s have been reported [5], [6], which shows that the architecture remains attractive for high-speed applications. Designs at these rates generally spend considerable effort on the comparator offset problem, for example through preamplification, averaging or interpolation [4]–[6].

Because the comparator is replicated $2^N - 1$ times, the choice between a continuous-time and a regenerative comparator sets the static power, the clock load and the speed of the whole array. For this reason, this work keeps the resistor ladder and the encoder identical and changes only the comparator.

B. StrongARM Latch Comparator Design

The StrongARM latch is a dynamic comparator in which an input differential pair, a clocked tail transistor and a cross-coupled regenerative pair are combined so that no static current flows once the decision has been made. The topology is closely related to the current-controlled latch sense amplifier of Kobayashi et al. [3], and its operation and the reasons for its wide use in high-speed ADCs are reviewed by Razavi [2].

Many variants have been proposed to improve its speed and its operation at low supply voltage. The double-tail latch of Schinkel et al. separates the input stage from the latch stage, so that the input pair can be biased for gain while the latch regenerates quickly, which gives a short setup-plus-hold time [7]. Babayan-Mashhadi and Lotfi later analyzed this structure and optimized it for low-voltage, low-power operation [8].

Two non-idealities are central to the comparison in this paper. The first is the input-referred offset, which results from the random mismatch of the input pair and, in a latch, also of the load and regeneration devices; the mismatch variance decreases with device area [9], and the effect of load capacitor mismatch on latch offset was analyzed in [10]. The second is kickback noise: the fast voltage swings on the internal nodes of a clocked latch couple back through the gate–drain capacitance of the input pair onto the input and reference nodes, which disturbs the resistor ladder and the preceding stage. Techniques to reduce kickback noise in latched comparators are presented in [11].

C. Continuous-Time (Op-Amp) Comparators

A comparator can also be realized as an open-loop op-amp that amplifies the input difference until the output reaches a logic level [1], [12]. Such a comparator needs no clock and is simple to design, but it draws static bias current, and its speed is limited by the gain–bandwidth product, the slew rate and the compensation of the amplifier [12]. In contrast to work that reports either comparator type alone, this paper evaluates both inside the same 3-bit Flash ADC under identical supply, process and simulation conditions.

III. FLASH ADC ARCHITECTURE AND COMPARATOR DESIGN

This section describes the 3-bit Flash ADC that is common to both designs and the two comparators placed inside it. The architecture is presented first, followed by the StrongARM latch comparator and the op-amp-based comparator.

A. 3-bit Flash ADC Architecture

The ADC consists of a resistor ladder of eight equal resistors ($R = 1\ k\Omega$) between $V_{REFL} = 0.6$ V and $V_{REFH} = 1.2$ V, which gives seven reference taps and

$$1\ LSB = (V_{REFH} - V_{REFL}) / 8 = 75\ mV \quad (1)$$

The ladder draws 75 µA, i.e., 45 µW from the 0.6 V reference span. Seven comparators compare the input V_{IN} with the taps (0.675, 0.750, 0.825, 0.900, 0.975, 1.050 and 1.125 V) and produce a thermometer code T_1–T_7, which a combinational encoder converts into the binary outputs $B_2B_1B_0$ [13]. With $'$ denoting the logical complement, the encoder equations are

$$B_2 = T_4 \quad (2)$$

$$B_1 = T_6 + T_2 \cdot T_4' \quad (3)$$

$$B_0 = T_7 + T_5 \cdot T_6' + T_3 \cdot T_4' + T_1 \cdot T_2' \quad (4)$$

The complete ADC is shown in Fig. 1.

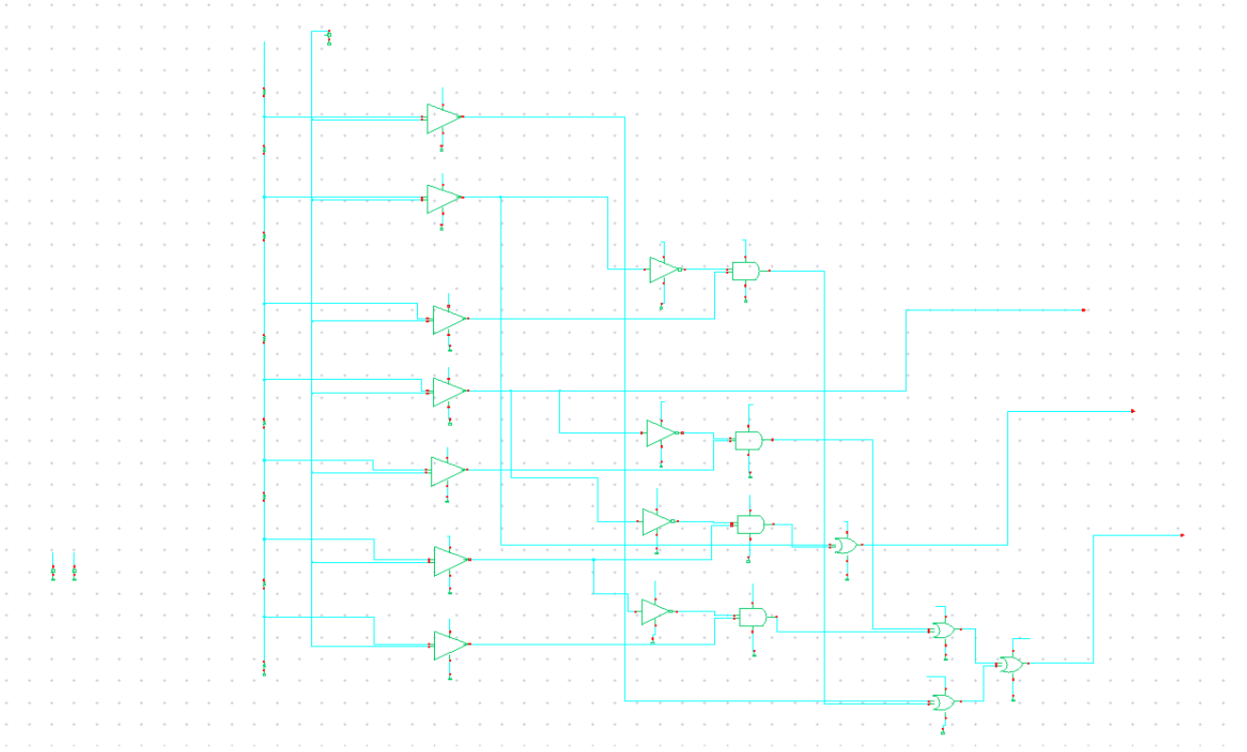

Fig. 1. Block diagram of the 3-bit Flash ADC

B. StrongARM Latch Comparator

The StrongARM comparator (Fig. 2) uses 15 transistors: a clocked tail transistor (NM4), an input differential pair (NM0, NM1), cross-coupled NMOS (NM2, NM3) and PMOS (PM0, PM1) pairs, four clocked PMOS reset switches (PM2–PM5), and two output inverters (PM6/NM5, PM7/NM6). When CLK is low, the internal nodes are precharged to V_{DD} and the outputs are reset. When CLK goes high, the tail turns on, the input pair discharges the internal nodes at different rates, and the cross-coupled pairs regenerate the difference to full swing [2]. All transistors have W = 2 µm and L = 180 nm

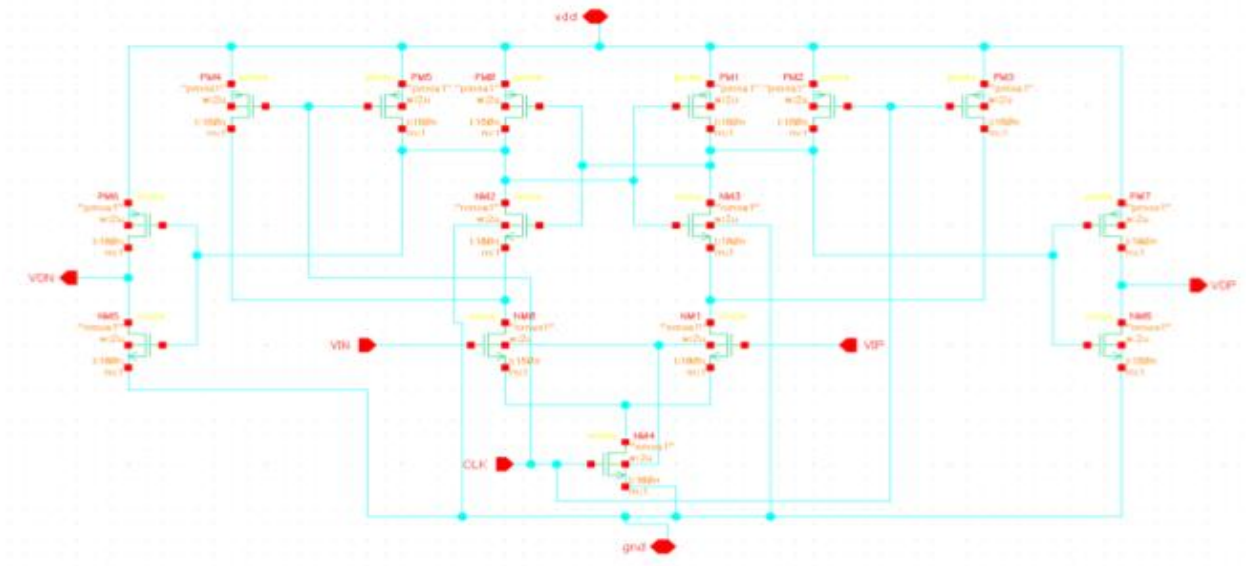

Fig. 2. StrongARM comparator schematic.

C. Op-Amp-Based Comparator

The conventional comparator (Fig. 3) is an open-loop differential op-amp with inputs VIN1 and VIN2, supplies V_{DD} and V_{SS}, and output VOUT. The output goes high when VIN1 exceeds VIN2 and low otherwise. It has no clock and no reset phase, so it resolves continuously and draws static bias current from V_{DD} at all times. The op-amp is a two-stage design using 11 transistors, with sizes given in Table I. A resistor-biased current mirror (R_0 = 340.32 kΩ, NM0, NM2, PM0, PM1) sets the bias; NM1 is the tail current source of the first stage, an NMOS differential pair (NM3, NM4) with a PMOS current-mirror load (PM4, PM5). The second stage is a common-source PMOS (PM3) with an NMOS current source (NM5). A 3 pF Miller capacitor (C_1) is connected from the first-stage output to VOUT, and the output drives a 10 pF load (C_0). The comparator draws about 11 µA from V_{DD} (about 20 µW at 1.8 V).

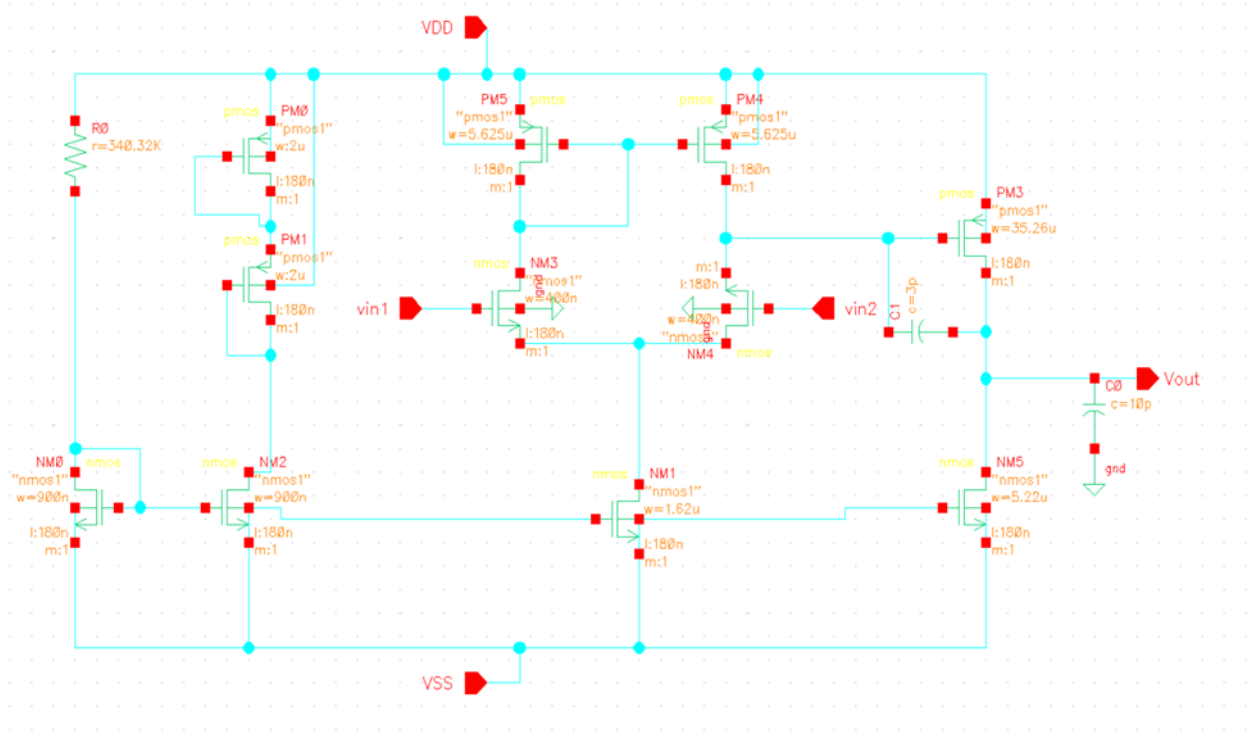

Fig 3 Op-amp-based comparator schematic.

TABLE 1. TRANSISTOR SIZES

Device	Comparator	W/L (µm)	Function
NM0, NM1	StrongARM	2/0.18	Input pair
NM2, NM3, PM0, PM1	StrongARM	2/0.18	Latch
NM4	StrongARM	2/0.18	Clocked tail
PM2–PM5	StrongARM	2/0.18	Reset switches
NM3, NM4	Op-amp	0.4/0.18	Differential pair
NM1	Op-amp	1.62/0.18	Tail current source
PM4, PM5	Op-amp	5.625/0.18	Active load
PM3	Op-amp	35.26/0.18	Second stage
NM0, NM2	Op-amp	0.9/0.18	Bias mirror
PM0, PM1	Op-amp	2/0.18	Bias branch
NM5	Op-amp	5.22/0.18	2nd-stage source
R0	Op-amp	340.32 kΩ	Bias resistor
C1 / C0	Op-amp	3 pF / 10 pF	Miller cap / load

IV. SIMULATION SETUP

Both ADCs were designed in Cadence Virtuoso and simulated with Spectre using the GPDK180 process design kit. Only the comparator differs between the two designs. All other conditions are identical, as listed in Table II, except the input ramp time, which is longer for the slower op-amp ADC.

TABLE I. SIMULATION CONDITIONS

Parameter	Value
Technology	GPDK180 (180 nm CMOS)
Supply voltage V_{DD}	1.8 V
Corner / temperature	tt / 27 °C
Ladder resistors	8 × 1 kΩ
V_{REFL} / V_{REFH}	0.6 V / 1.2 V
LSB	75 mV
Clock frequency (StrongARM)	100 MHz
Clock duty cycle / rise time	50 % / 100 ps
Input signal	Ramp, 0.6–1.2 V in 1 µs (StrongARM) / 1 ms (op-amp)
Monte Carlo runs	200

The following metrics were evaluated: (i) functional check of the output codes; (ii) DNL and INL from the code transition points; (iii) average power from the supply current; (iv) propagation delay (CLK-to-output for the StrongARM, input-crossing-to-output for the op-amp) at differential inputs of 37.5, 75 and 150 mV; (v) maximum clock frequency at which all eight codes are correct (for the clockless op-amp ADC, the maximum input rate at which they are correct); (vi) input-referred offset by Monte Carlo analysis with process and mismatch variation; (vii) kickback noise on the input and reference nodes; and (viii) transistor count.

V. RESULTS AND DISCUSSION

This section presents the simulation results of the two ADCs. Functional verification is shown first, followed by static performance, power consumption, speed, and a summary comparison.

A. Functional Verification

Figs. 4 and 5 show V_{IN} and the outputs $B_2B_1B_0$ (D2 D1 D0) for both ADCs, and CLK for the StrongARM ADC. The output code steps from 000 to 111 without missing or repeated codes. For the StrongARM ADC, each code lasts about 125 ns (about 12 clock cycles at 100 MHz), so the output updates at every rising clock edge with one-cycle latency. The op-amp ADC follows the input continuously but with a delay of about 12 µs, so a slower 1 ms ramp (about 125 µs per code) is used for it.

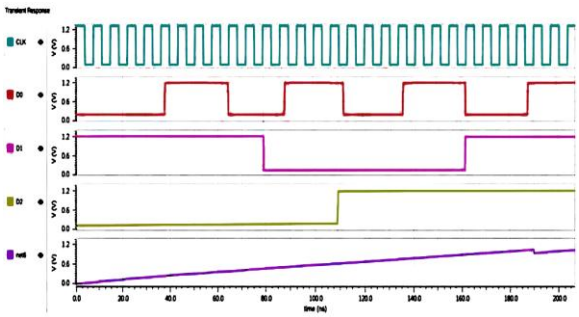

Fig 4Transient waveforms of the StrongARM-based ADC (CLK, D0, D1, D2 and V_{IN}).

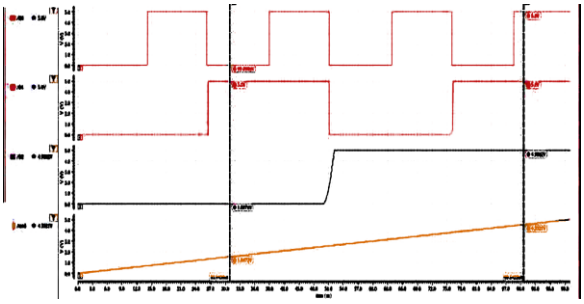

Fig 5 Transient waveforms of the op-amp-based ADC (D0, D1, D2 and V_{IN}).

more because its input pair is very small (400 nm/180 nm), so its mismatch offset ($\sigma \approx 20$ mV) is larger than that of the StrongARM ($\sigma \approx 9$ mV), consistent with the area dependence of device matching [9]. The DNL and INL at each code transition are plotted in Fig. 6.

B. Static Performance (DNL/INL)

The measured code transition voltages are listed in Table III. The maximum DNL and INL are 0.31/0.19 LSB for the StrongARM ADC and 0.63/0.37 LSB for the op-amp ADC. Both stay below 1 LSB, so no code is missing, but the op-amp ADC comes close to the ±0.5 LSB limit. Its transitions deviate reference nodes; and (viii) transistor count. DNL and INL are computed as

$$DNL(k) = [T(k+1) - T(k)] / LSB - 1 \quad (5)$$

$$INL(k) = [T(k) - T_{ideal}(k)] / LSB \quad (6)$$

where T(k) is the input voltage at the kth code transition.

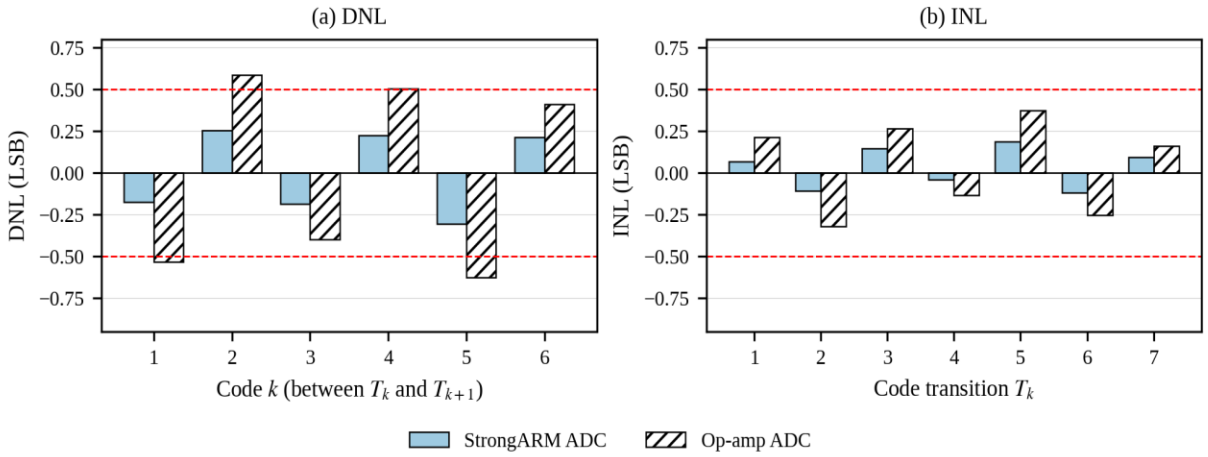

Fig 6 DNL and INL of the StrongARM-based and op-amp-based Flash ADCs, computed from the code transition voltages of Table III The dashed lines mark ±0.5 LSB.Code Transition Voltages

Transition	Ideal (V)	StrongARM (V)	Op-amp (V)
T_1	0.675	0.680	0.691
T_2	0.750	0.742	0.726
T_3	0.825	0.836	0.845
T_4	0.900	0.897	0.890
T_5	0.975	0.989	1.003
T_6	1.050	1.041	1.031
T_7	1.125	1.132	1.137

C. POWER CONSUMPTION

Table IV lists the average power, where SA denotes StrongARM and "comp." the comparator bank (seven comparators); the totals include the 45 µW ladder and the encoder. The op-amp has no clock, so its power is independent of f_{clk}. The op-amp bank draws 7 × 20 µW = 140 µW of static bias power at all times (about 11 µA per comparator from V_{DD}). The StrongARM has no static current, so its power is purely dynamic (CV_{DD}^2f) and grows almost linearly with clock frequency, from 60 µW at 50 MHz to 232 µW at 200 MHz (about 1.2 µW/MHz for the bank). At 100 MHz, the StrongARM bank uses about 16 % less power than the op-amp bank (118 versus 140 µW), and the ADC totals differ by about 8 % (172 versus 186 µW). The StrongARM total overtakes the op-amp total at roughly 110 MHz, but the op-amp can convert only at a few tens of kilohertz, so its energy per conversion is thousands of times higher.

TABLE II. AVERAGE POWER (µW)

f_{clk}	SA comp.	SA total	Op-amp comp.	Op-amp total
50 MHz	60	110	140	186
100 MHz	118	172	140	186
200 MHz	232	294	140	186

D. Speed: Delay and Maximum Sampling Frequency

The comparator delays are listed in Table V. The maximum clock frequency at which all eight codes remain correct is 800 MHz for the StrongARM ADC and 40 kHz (maximum input rate) for the op-amp ADC. The StrongARM regenerates exponentially through positive feedback, so it resolves in a few hundred picoseconds even for LSB/2 inputs. The open-loop op-amp is limited by slew: its output falls only as fast as the NM5 current source (about 1 µA) can discharge the 10 pF load and the 3 pF Miller capacitor, which gives delays of about 10 to 12 µs. The Miller capacitor is not needed in an open-loop comparator; removing it and reducing the load to a realistic encoder load (tens of femtofarads) should bring the delay down to a few nanoseconds. Both delays increase as the differential input shrinks (metastability region for the latch, slow overdrive recovery for the op-amp).

TABLE III. COMPARATOR DELAY

Differential input	StrongARM (ps)	Op-amp (µs)
37.5 mV (LSB/2)	280	12
75 mV	230	11
150 mV	190	10

E. Summary Comparison

Table VI summarizes the overall comparison of the two ADCs.

TABLE IV. OVERALL COMPARISON

Metric	StrongARM ADC	Op-amp ADC
Technology / V_{DD}	GPDK180 / 1.8 V	GPDK180 / 1.8 V
Transistors per comparator	15	11
Comparator transistors (×7)	105	77
Comparator power (µW)	118	140
Total ADC power (µW)	172	186
Delay at LSB/2	280 ps	12 µs
Max. clock frequency	800 MHz	40 kHz
Max. DNL / INL (LSB)	0.31 / 0.19	0.63 / 0.37
Offset σ (mV)	9	20
Kickback peak (mV)	35	2

VI. CONCLUSION

A 3-bit Flash ADC was designed in 180 nm CMOS using two different comparators, and the two versions were compared under identical conditions. The StrongARM-based ADC showed lower power by about 8 % at 100 MHz (172 versus 186 µW), higher speed by more than four orders of magnitude (800 MHz versus 40 kHz; 280 ps versus 12 µs delay) and about 50 % smaller transistor gate area (about 5.4 μm^2 versus 10.8 μm^2 per comparator, although it uses more transistors: 15 versus 11). The area advantage becomes larger once the 3 pF compensation capacitor and the 340 kΩ bias resistor of the op-amp are counted. Its offset σ was also lower, 9 mV against 20 mV for the op-amp design.

The StrongARM ADC suits high-speed, low-power applications that can handle kickback with buffered references; the op-amp ADC in its present form suits only very low-speed use, and its speed would improve strongly if the compensation capacitor and the 10 pF load were removed. These results are pre-layout, with no parasitics and a single process corner (tt, 27 °C). Future work includes layout and post-layout simulation, offset calibration, and extension to higher resolution.

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